New-Generation of Trench-Assisted Planar SiC MOSFETs

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17-22nd, September 2023
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## Broadest SiC MOSFET Portfolio

<table>
<thead>
<tr>
<th>Resistance (mΩ)</th>
<th>600 V</th>
<th>750 V</th>
<th>1200 V</th>
<th>1700 V</th>
<th>2200 V</th>
<th>3300 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000 mΩ</td>
<td>* 1000 mΩ</td>
<td>* 1000 mΩ</td>
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</tr>
<tr>
<td>500 mΩ</td>
<td>* 450 mΩ</td>
<td>* 295 mΩ</td>
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</tr>
<tr>
<td></td>
<td>* 135 mΩ</td>
<td>* 160 mΩ</td>
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<tr>
<td>100 mΩ</td>
<td>* 60 mΩ</td>
<td>* 75 mΩ</td>
<td>* 64 mΩ</td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>* 45 mΩ</td>
<td>* 45 mΩ</td>
<td>* 40 mΩ</td>
<td>* 45 mΩ</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>* 34 mΩ</td>
<td>* 34 mΩ</td>
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</tr>
<tr>
<td></td>
<td>* 25 mΩ</td>
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<td>* 25 mΩ</td>
<td>* 25 mΩ</td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>* 20 mΩ</td>
<td>* 20 mΩ</td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>* 17 mΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 mΩ</td>
<td>* 10 mΩ</td>
<td>* 10 mΩ</td>
<td>* 12 mΩ</td>
<td>* 10 mΩ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **60+ SiC MOSFET products**
- **Discrete**
- **Bare Die**
- **Power Modules**

*Note (1): based on GeneSiC voltage range of production released SiC MOSFETs compared to all publicly identified voltage ranges of other SiC suppliers.*
GeneSiC leads in Performance, Ruggedness, and Reliability

- Traditional designs using planar or trench techniques, which must compromise between manufacturability, performance, and/or reliability.
- GeneSiC trench-assisted planar-gate technology enables leading-edge performance with high-yielding manufacturing.

G3R40MT12K
1200V 40mΩ TO-247-4

22kW OBC + 3kW DC-DC Combo
Bi-Directional; SiC-based 1-ϕ & 3-ϕ Compatibility

>95% Efficiency @ Full Load

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New-Generation 750 V SiC MOSFETs

- T5 mm x 5 mm chips with (optional) solderable top metal
- Extremely tight $R_{DS(ON)}$ (10 mOhm) and $V_{TH}$ (3.0 V) distributions across wafers
HTGB @ Vgs+22 V, 175°C

- Vgs +22 V stress applied at 175°C
- Less than 3% $V_{TH}$ variation observed after 540 hours
HTRB @ 750 V, 175°C

- Minimal Idss or $V_{TH}$ shift observed during 750 V/175°C HTRB stress
HTRB @ 800 V, 175°C

• Excellent parameter stability observed even under accelerated HTRB stress
HV-HAST @ 600 V, 130°C, 85% RH

- Excellent robustness of key parameters under 96 hour accelerated humidity stress conditions
Discover more at navitassemi.com