Gate-Driver IC Selection Guidelines for GeneSiC MOSFETs

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Navitas' GeneSiC silicon carbide (SiC) MOSFETs enable high-efficiency power delivery for a variety of applications, such as electric-vehicle fast charging, data center power supplies, renewable energy, energy storage systems, industrial and grid infrastructure. With significantly higher efficiency and faster switching than legacy silicon MOSFETs and insulated-gate bipolar transistors (IGBTs), SiC MOSFETs gate-drive requirements must be considered carefully during the design process. This application note covers the critical parameters when choosing a gate-driver IC for SiC MOSFETs.

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1. Gate-Drive ICs: Critical Parameters

Several important factors must be considered when selecting a gate-driver IC for SiC MOSFETs. Some examples of these are:

- I. Maximum gate driver supply voltage
- II. UVLO selection
- III. CMTI capability
- IV. Isolation voltage
- V. Drive current
- VI. Active miller clamp
- VII. Short-circuit protection

I. Maximum gate driver supply voltage

SiC MOSFETs often require a higher gate driving voltage compared to their silicon counterparts. Different technologies and generations of SiC MOSFETs can also impact the recommended gate driving voltages. In GeneSiC's case there are currently two active generations of SiC MOSFETs noted by the prefixes G2R (2nd generation) and G3R (3rd generation). For optimal performance, the G2R MOSFETs are recommended to be driven at a higher gate voltage compared to the G3R MOSFETs. The recommended gate driving voltages for GeneSiC MOSFETs can be seen in Tables 1 and 2 below.

Table 1 Recommended gate-source voltage value from a datasheet of a G2R GeneSiC MOSFET

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)				
Gate-Source Voltage (Static)	$V_{GS(op)}$	Recommended Operation	-5 / +20	V

Table 2 Recommended gate-source voltage value from a datasheet of a G3R GeneSiC MOSFET

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)				
Gate-Source Voltage (Static)	$V_{GS(op)-ON}$ $V_{GS(op)-OFF}$	Recommended Operation	+15 to +18 -5 to -3	V	Note 1

Here, $V_{GS(op)-ON}$ is the recommended on-state gate voltage of the SiC device and $V_{GS(op)-OFF}$ is the recommended off-state gate voltage. In many applications, a negative gate voltage is recommended to reduce the possibility of shoot-through due to the Miller effect.

The selected gate driver IC must support the chosen gate voltages. The requirement for the maximum supply voltage of the gate driver IC (V_{cc_max}), is denoted by the following calculation:

$$V_{cc\_max} > \left|V_{GS(op)-ON}\right| + \left|V_{GS(op)-OFF}\right|$$

An example gate-source voltage for a G3R GeneSiC MOSFET is shown in Figure 1 below.
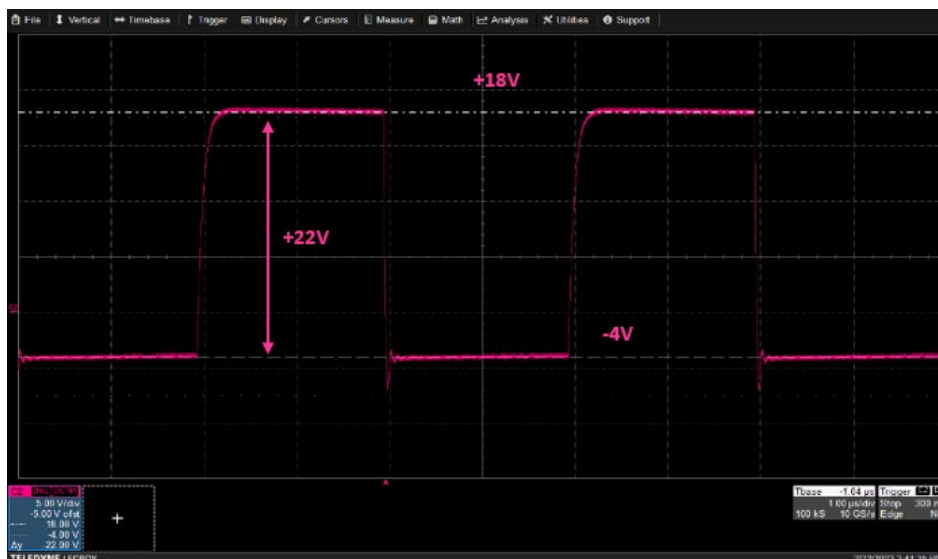
Fig. 1:   Gate to source voltage waveform for 3rd generation GeneSiC MOSFET

In this example, the MOSFET is being driven with +18 V and -4 V. As a result, the selected gate driver IC in this example must have a V_{cc_max} specification of greater than 22 V.

II.   UVLO selection

Undervoltage lockout (UVLO) is an important consideration when selecting a gate driver for SiC MOSFETs. UVLO protection is implemented in gate drivers to prevent the gate voltage from dropping under a certain threshold. This is a key feature that protects the system in the case of a bias supply failure. In isolated gate drivers, a bias voltage is provided for both the primary (signal side) and the secondary (power side) of the gate driver. In this case, the secondary UVLO setting will determine the minimum gate drive voltage for the MOSFET.

Figure 2 shows an example of the output characteristics of a SiC MOSFET (G3R75MT12J). It can be seen from Figure 2 that the saturation current depends on the applied gate voltage. A lower on-state gate voltage will cause the MOSFET to saturate at a lower drain current. Choosing an appropriate UVLO setting for the gate drive IC will prevent the MOSFET from entering the saturation region and thereby protecting the system.

Figure 3 shows the dependency of the on-state resistance ($R_{DS(ON)}$) of the G3R75MT12J on the applied gate voltage. The typical $R_{DS(ON)}$ of this MOSFET is 75 mΩ at 25 °C and 15 V at the gate. If the gate voltage drops to 12 V, the $R_{DS(ON)}$ will increase by approximately 40%. This same trend is observed at higher junction temperatures although the $R_{DS(ON)}$ increase will be lower. This curve shows the importance of selecting the right gate voltage to optimize the conduction loss of the MOSFET. An appropriate UVLO setting will limit the operation of the MOSFET to the more efficient region of the curve and thereby optimizing the efficiency of the system and ensuring lower junction temperatures in the MOSFET.
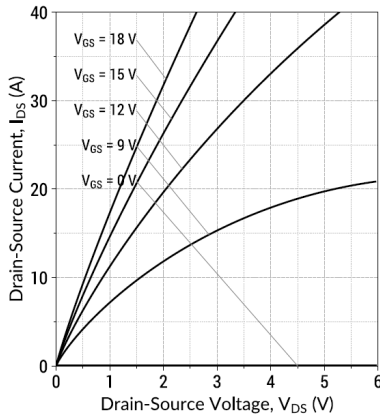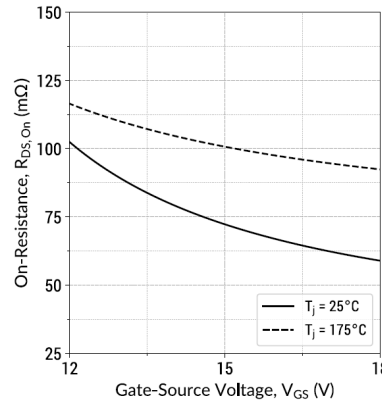
Fig. 2: I-V curve for G3R75MT12J

Fig. 3: On-state resistance vs. Gate voltage for G3R75MT12J

Choosing an appropriate UVLO setting is important for a safe and efficient MOSFET operation. Typically, a UVLO setting of 12 V or higher is recommended for SiC MOSFETs.

III. CMTI capability

Common-mode Transient Immunity (CMTI) is a critical parameter for selecting isolated gate drivers. CMTI is defined as the maximum allowable slew rate of the common mode voltage applied between two isolated circuits. As a rule of thumb, for an isolated gate driver, the CMTI rating should be greater than the maximum switching speed of the MOSFET in the application circuit. If this rating is exceeded, the output of the gate driver can see different fault scenarios such as a missing pulse, excessive propagation delay, false output state or latched output. Some of these failure modes can potentially be destructive. Since SiC MOSFETs can switch much faster than Si MOSFETs and IGBTs, special consideration should be taken to select an isolated gate driver with a sufficiently high CMTI rating for the target application.

Typically for high efficiency applications, fast switching speeds in excess of 50 V/ns can be reached and therefore, an isolated gate driver with a CMTI rating of 100 V/ns or higher is recommended.

IV. Isolation voltage

Isolation is defined as the electrical separation between different circuits in a system such that no direct conduction path will exist between them. Signals can still pass through the isolation barrier by using different isolation technologies such as: capacitive, magnetic, or optical. Isolation requirements are evaluated on a system level and will depend on the safety requirements and the applicable standards. For some applications, such as those where the controller lies in a different domain compared to the MOSFETs being driven, an isolator is needed. Oftentimes, an isolated gate driver will be considered for these applications because it lowers the number of components and can simplify the PCB layout. In this case, careful consideration should be given to the system level isolation requirements when selecting the gate driver.

Different applications require different isolation voltage ratings for gate-driver ICs. This rating depends on the working voltage, and isolation requirement (functional/basic/reinforced) amongst other factors.

Typically, several isolation voltage levels are available, from 1 kV$_{RMS}$ to 5.7 kV$_{RMS}$. The designer should select an isolator or isolated gate driver with the appropriate ratings to meet their isolation needs according to their application.

V.   Gate drive current

Source and sink currents are the maximum currents that the gate driver can supply during turn-on and turn-off respectively. To switch the MOSFET with desired switching speed, it is important to select a gate driver with the correct drive current capability. A typical driving circuit is shown in Figure 4.
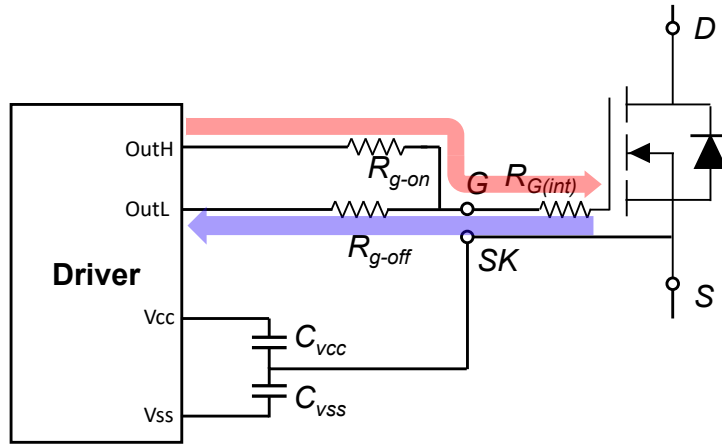
Fig. 4:   Typical driving circuit of a SiC device

The required I_{g_on} (source current) and I_{g_off} (sink current) during turn-on and turn-off can be calculated by the equation shown below.

$$I_{g\_on} = \frac{\Delta V_{gs}}{R_{g-on} + R_{G(int)} + R_{g-drv-on}}$$

$$I_{g\_off} = \frac{\Delta V_{gs}}{R_{g-off} + R_{G(int)} + R_{g-drv-off}}$$

Where ΔV_{gs} is the voltage applied across the gate-to-source terminals of the SiC MOSFET, which can be calculated by:

$$\Delta V_{gs} = \left|V_{GS(op)-ON}\right| + \left|V_{GS(op)-OFF}\right|$$

R_{g-on} and R_{g-off} are the external turn-on and turn-off gate drive resistors respectively.

$R_{G(int)}$ is the internal gate resistor of SiC MOSFET, which can be found in the datasheet. For example, the $R_{G(int)}$ of G3R40MT12J is 1.2 Ω as shown in Table 3 below. Smaller $R_{G(int)}$ values are a competitive advantage for GeneSiC MOSFETs compared to other devices in the market.

Table 3:   Internal gate resistor value of G3R40MT12J shown in the datasheet.

Internal Gate Resistance	$R_{G(int)}$	f = 1 MHz, V$_{AC}$ = 25 mV	1.2	Ω

$R_{g\text{-drv-on}}$ and $R_{g\text{-drv-off}}$ are the internal turn-on and turn-off resistors of the gate driver. Not all vendors provide this value in their datasheet. However, these values are usually much smaller compared to $R_{g\text{-on}}$, $R_{g\text{-off}}$ and $R_{G(int)}$ and therefore can be ignored when approximating the drive current requirement.

Using G3R40MT12J as an example, the recommended turn-on and turn-off gate-to-source voltages are +18 V and -3 V. With 6.8 Ω $R_{g\text{-on}}$ and 3.3 Ω $R_{g\text{-off}}$ as the external gate resistors, the required source and sink gate currents, respectively, can be calculated as shown below:

$$I_{g-on} = \frac{18\ V + 3\ V}{6.8\ \Omega + 1.2\ \Omega} = 2.6\ A$$

$$I_{g-off} = \frac{18\ V + 3\ V}{3.3\ \Omega + 1.2\ \Omega} = 4.7\ A$$

To make sure that turn-on and turn-off speeds can still be controlled by the external resistors, the source and sink current capabilities of the gate driver in this case should be greater than 2.6 A and 4.7 A respectively. Otherwise, the gate driver IC becomes the limiting factor for the switching speed.

An example of how the gate driver IC's driving capability impacts the switching speed is shown below. Here, the device under test is the G3R40MT12J. The driving capabilities of the two gate drivers (Si8275 and SLMi8233) used for this test are shown in Table 4.

Table 4:   Driving capability of SI8275 and SLMi8233

Part No.	Source Capability	Sink Capability
SI8275	1.8 A @15 V	4 A @15 V
SLMi8233	4 A @15 V	6 A @15 V

SLMi8233 has a higher source current capability and therefore faster turn-on speeds can be achieved using this part compared to the SI8275. This is demonstrated in the experimental results shown in Figure 5. At 30 A turn-on current, when using a 1.8 Ω resistor for R_{g-on} for both gate drivers, 42 V/ns and 4.2 A/ns switching speeds can be achieved using the Si8275 compared to 48 V/ns and 8.6 A/ns when using SLMi8243.

However, when we increase the external gate resistance, the difference becomes smaller since the gate driver's capability is no longer the limitation, as shown in Figure 6.
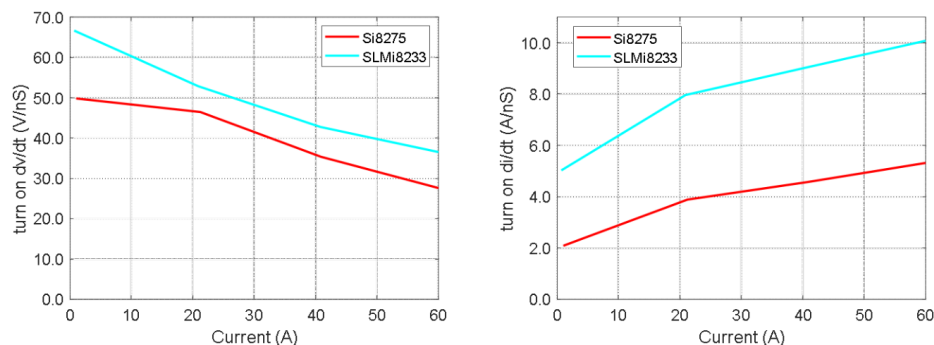
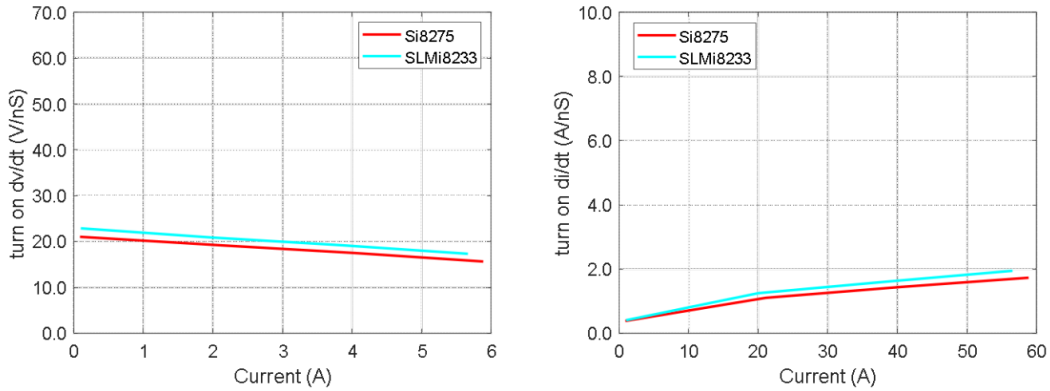Fig. 5:   Turn-on dV/dt and di/dt comparison between SI8275 and SLMi8243 @1.8 Ω R_{g-on}

Fig. 6:   Turn-on comparison between Si8275 and SLMi8243 @20Ω $R_{g\text{-}off}$

VI.   Active Miller clamp

In bridge topologies, high switching speeds can cause voltage spikes to appear on the gate due to the induced current flowing through the Miller capacitor of the MOSFET. This effect is demonstrated in a boost converter in Figure 7 below.
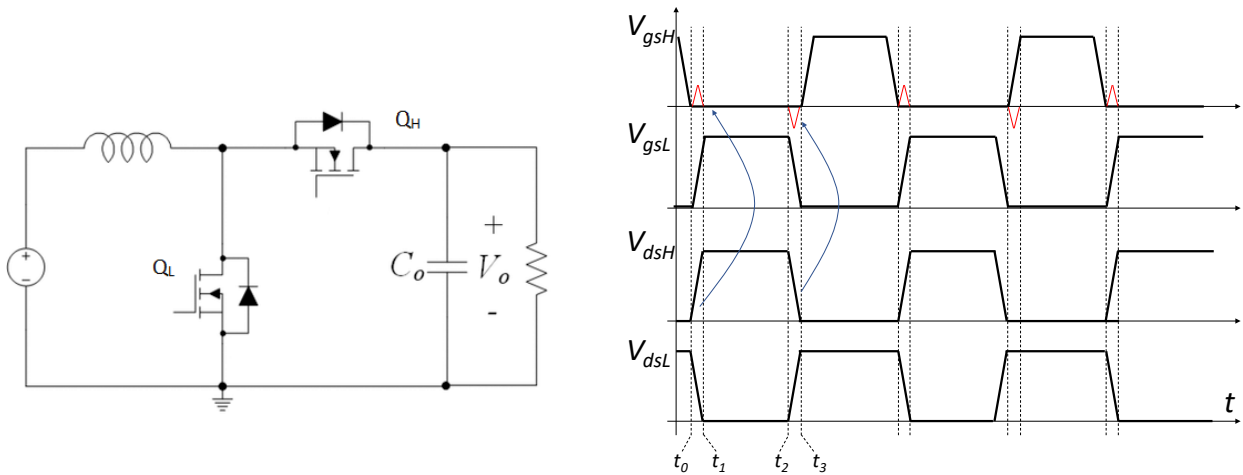

Fig. 7:   Miller capacitor induced gate-to-source voltage bounce.

During t_0-t_1, when the Q_L is turning-on, there will be a positive *dv/dt* on the V_{DS} of the freewheeling device (Q_H). As a result, a parasitic current will be generated from the drain to the gate through C_{gd} (Miller capacitor). The voltage drop caused by this current on the gate resistor shows on the gate terminal and causes the voltage bounce, as shown in Figure 8.
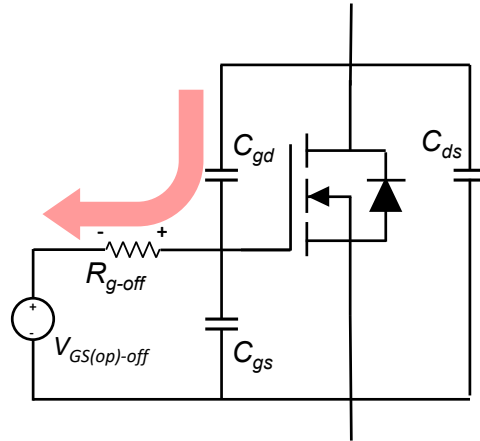
Fig. 8: Miller capacitor induced gate-to-source voltage bounce

The peak of the induced voltage bounce can be calculated by,

$$V_{gs} = V_{GS(op)-OFF} + R_{g-off}C_{gd}\frac{dv}{dt}$$

From this equation, faster switching speeds, or larger C_{gd} or larger R_{g-off} can generate a higher voltage bounce. If the peak of this voltage bounce exceeds the threshold voltage, the MOSFET can falsely turn-on which risks a shoot-through condition.

It can also be seen from the above equation that a negative off-state gate voltage ($V_{GS(op)-OFF}$) can mitigate the parasitic turn-on issue by increasing the safety margin from the off-state voltage of the gate to the threshold voltage.

Another way that this issue can be mitigated is by using an active Miller clamp (Figure 9).
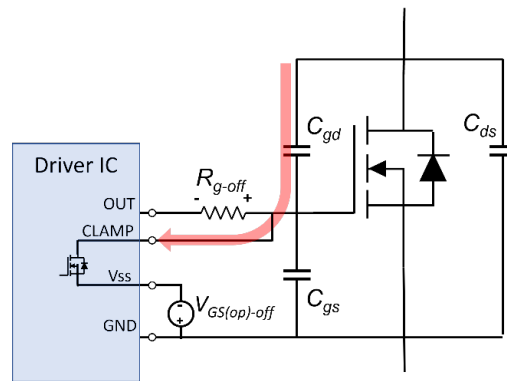
Fig. 9: Gate driver with miller clamp circuit

The active Miller clamp provides a lower impedance path after the device is turned off. Therefore, R_{g-off} in the above equation is bypassed and instead, the induced Miller current goes through a significantly lower impedance path which creates a much smaller voltage bounce thereby mitigating the risk of a false turn-on. It is important to follow best layout practices for the gate driver IC to reduce the parasitic inductance of the driving loop and to ensure that the Miller clamp will operate effectively.

VII. Short-circuit protection

SiC MOSFETs have stringent short circuit protection requirements as compared to Si MOSFETs and IGBTs. As a result, for some applications, a fast and reliable short circuit protection circuit is needed to ensure a robust system operation.

The most-commonly used short-circuit protection method, which is available in many gate drivers, is desaturation detection (DESAT). The DESAT circuit senses the on-state drain-source voltage and uses this to prevent the device from entering the deep saturation region.

The response time of the DESAT circuit is comprised of three components:

1. Blanking time or DESAT detection time
2. The delay between the DESAT detection and the beginning of the gate shutdown
3. Shutdown time during which the gate is pulled low

Most gate drivers SiC MOSFETs can start shutting down the MOSFET 500 ns after DESAT detection. For SiC MOSFETs, it is recommended that the first two components of the DESAT response time (i.e. the time it takes from the beginning of the short circuit event until the time the gate voltage starts decreasing) take less than 1 µs.

A typical DESAT circuit is shown in Figure 10.
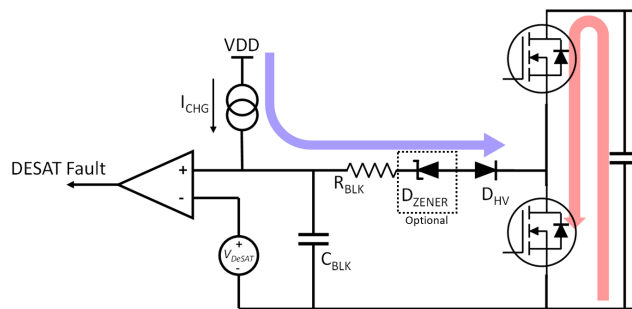
Fig. 10:   Typical desaturation circuit

The circuit consists of a blanking resistor (R_{BLK}), a blanking capacitor (C_{BLK}), and a high voltage diode (D_{HV}). When the active device is off, the drain-source voltage is as high as the bus voltage, and D_{HV} is blocking. When the device turns on, a current source charges the blanking capacitor, and D_{HV} is forward biased and conducts. During normal operation, the capacitor voltage is clamped to the drain-to-source voltage of the device.

During a short circuit event, a large current will flow through both high side and low side devices which causes a significant rise of the drain-source voltage. This charges capacitor (C_{BLK}) to the threshold voltage (V_{DESAT}), which triggers the comparator to shut down the device.

The drain-source voltage which triggers the desaturation protection can be calculated by,

$$V_{ds-sat} = V_{DeSAT} + V_{f-HV}$$

Where V_{DESAT} is the threshold voltage and $V_{f\text{-}HV}$ is the forward voltage-drop of D_{HV} and R_{BLK}. For some gate drivers, the threshold voltage V_{DESAT} cannot be adjusted. To have some controllability for the protection threshold, a Zener diode can be used in series with D_{HV}. Then the drain-source voltage that triggers the desaturation protection can be calculated by,

$$V_{ds-sat} = V_{DeSAT} + V_{f-HV} + V_{Zener}$$

Where V_{Zener} is the breakdown voltage of the Zener diode.

The capacitor C_{BLK} and can also be used to adjust the blanking time, during which the desaturation protection will not respond. The blanking time is calculated as:

$$t_{BLK} = \frac{C_{BLK}V_{DeSAT}}{I_{CHG}}$$

2.   Gate-Driver IC Selection

A non-exhaustive list of recommended isolated gate driver ICs is shown in Table 5.

Table 5:   Sample of Recommended Isolated Gate Driver ICs for SiC MOSFETs

Manufacturer	Part No.	No. Chan.	V$_{CC}$ max (V)	UVLO typ. (V)	CMTI typ. (V/ns)	Source Capability (A)	Sink Capability (A)	Miller Clamp	DESAT	Isolation Voltage (UL1577) (kV)
ADI	ADUM4146	1	30	11.5/14.5	100 (min)	11	9	Y	Y	5
Novosense	NSi6601		32	9.2/13.2	150 (min)	5	3	Y	N	3/5.7
Sillumin	SLMi335		40	11.6	150 (min)	4	4	N	Y	5
Skyworks	Si827x		30	3/5/8/12	300	1.8	4	N	N	2.5
	Si823Hx		30	6/8/12	125 (min)	4	4	N	N	5
	Si828x		30	9/12/13/15	125 (min)	2.7	5.5	Y	Y	3.75/5
TI	UCC21755		33	12	150 (min)	10	10	Y	Y	5.7
	UCC23511		33	8.5/12.5	150 (min)	1.5	2	N	N	5.7
	UCC23513		33	14	150 (min)	4.5	5.3	N	N	5.7
ADI	ADUM4221	2	35	4.4/7.3/11.3	150	8	8	N	N	5.7
Novosense	NSi6602		25	6.2/8.5/13.2	150	4	6	N	N	2.5/3/5.7
Sillumin	SLMi824x		40	8.5/12.5	100 (min)	4	7	N	N	2.5/5
Skyworks	Si827x		30	3/5/8/12	300	1.8	4	N	N	1/2.5
	Si823Hx		30	6/8/12	125 (min)	4	4	N	N	2.5/5
	Si8252x		30	5/8/12	125 (min)	4	4	N	N	2.5/5
TI	UCC21530		25	8.5/13.5	100 (min)	4	6	N	N	5.7

For some gate driver part numbers, there are different available suffixes to select different configurations such as UVLO levels, number of channels, isolation voltage, etc. However, the most important and relevant parameters are listed above table.

For questions regarding compatibility on gate drivers that are not listed in Table 5, you can reach out to Info@NavitasSemi.com. For SiC device selection, electrical and mechanical models, please refer to https://genesicsemi.com/

Additional Information