PCB Layout Recommendations for GeneSiC MOSFETs

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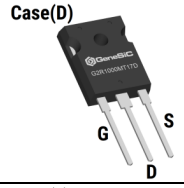
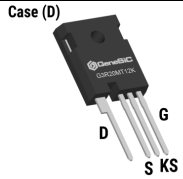
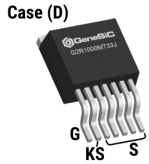
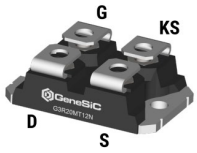
1. Introduction

Silicon Carbide (SiC) MOSFETs have gained a lot of popularity in the power electronics field due to their compelling advantages over their silicon counterparts. SiC MOSFETs enable higher power density and higher efficiency designs and therefore, are widely used in some applications including renewable energy systems, electric vehicle chargers and traction inverters, industrial motor drives and aerospace electronics. In order to harness the full potential of SiC MOSFETs, careful consideration of their unique electrical properties is required during printed circuit board (PCB) layout and design. This application note delves into the critical aspects of PCB layout recommendations for Navitas' GeneSiC SiC MOSFETs, offering insights to optimize performance, minimize parasitic effects, and ensure reliable operation.

2. Discrete SiC MOSFET packages

GeneSiC MOSFETs come in the following packages shown in Table 1. The recommended footprint for each part can be found in the "Recommended Solder Pad Layout" section of the datasheet. An example footprint is shown for G3R60MT07J in Figure 1.

Table 1- GeneSiC MOSFET Packages

Package Name	Package Photo	Part Number Suffix
TO-247-3		D
TO-247-4		K
TO-263-7		J
SOT-227		N

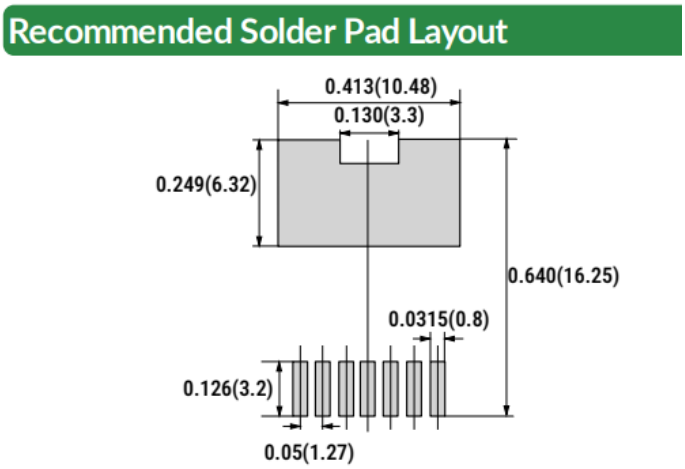
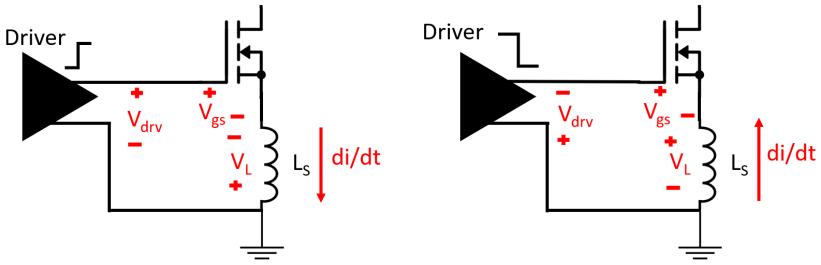


Figure 1 - Recommended Solder Pad Layout for G3R60MT07J

All discrete MOSFETs have a 'Drain', 'Source' and 'Gate' terminal. Except for MOSFETs in the TO-247-3 package, where a fourth terminal 'Kelvin Source' (KS) is also offered. The inclusion of the KS pin offers several benefits which will be discussed further in the following section.

Benefits of the Kelvin Source Pin

The Kelvin Source pin (KS) can have a significant impact on performance. In a three terminal MOSFET, the high source inductance (L_S) can limit the switching speed. Figure 2 shows a simplified diagram for the switching transitions in a 3 terminal MOSFET. During the turn-on transient, a positive voltage (V_{drv}) is provided by the driver to charge the gate-to-source capacitor. As the MOSFET turns on and starts conducting current a negative voltage is formed across L_S and this voltage will reduce the effective gate-to-source voltage (V_{GS}) during the turn-on transition which will slow down the switching speed and increase the switching loss. The inverse can also be observed during the turn-off transient.



a) Turn-on transient b) Turn-off transient

Figure 2 - Switching Transitions in a 3 Terminal MOSFET

This magnitude of induced source inductance voltage (V_L) depends on the slew rate of the MOSFET current (di/dt) as well as the magnitude of L_S.

In contrast, for MOSFETs with a KS pin, the source inductance is not part of the gate loop and therefore any voltages induced across this inductance does not counteract the driver voltage (Figure 3). This enables 4-terminal MOSFETs to achieve faster switching and lower switching losses.

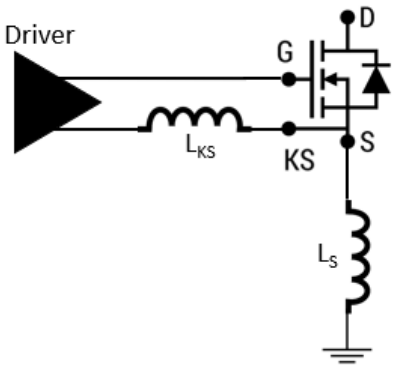


Figure 3 - Simplified gate loop of 4-terminal MOSFET

Figure 4 shows a switching loss comparison between MOSFETs that have identical dies but one of the MOSFETs is packaged in a TO-247-4 package with a Kelvin Source pin while the other is packaged in a TO-247-3 package. The two MOSFETs were tested under the same conditions and as expected from the analysis above, the TO-247-4 packaged MOSFET has a superior switching performance both in the turn-on and turn-off transients.

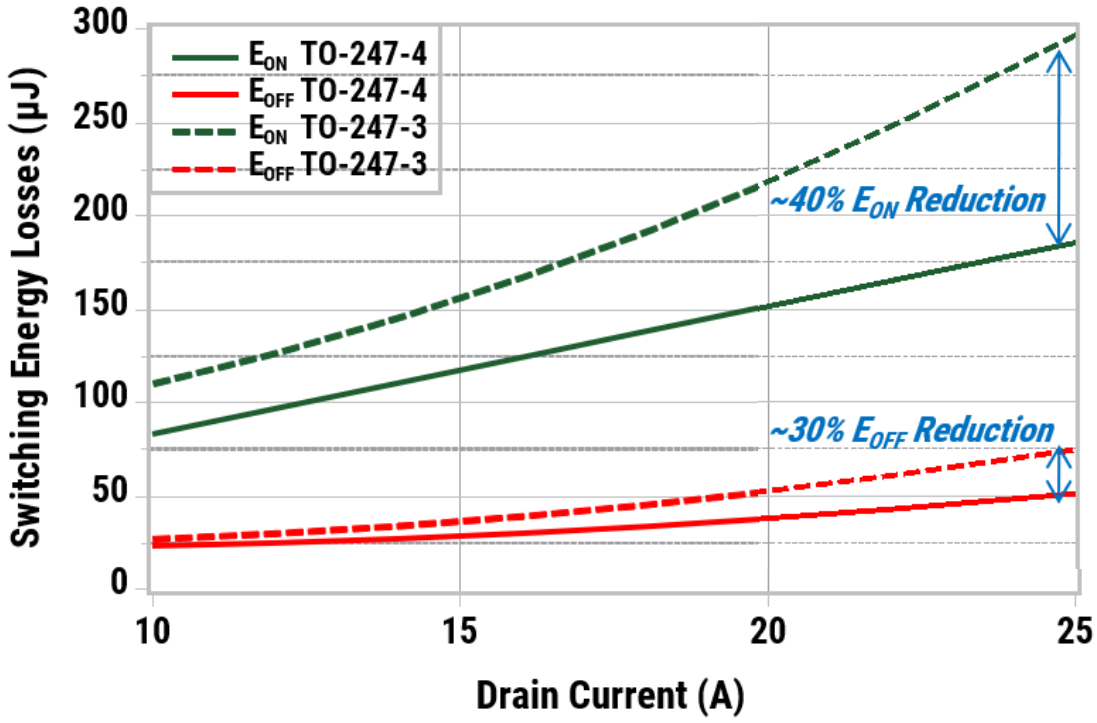


Figure 4 - Switching Loss Comparison between 3-terminal and 4-terminal MOSFET

In the following sections, the PCB layout guidelines for GeneSiC MOSFETs will be provided both in terms of the gate-loop and power-loop.

3. Gate-Loop Layout

The gate-driving loop is formed by the C_{GS} of the SiC device, turn-on/turn-off resistors (R_{GON} and R_{GOFF}), gate driver decoupling capacitors (C_{VDD} and C_{VSS}) and the gate loop inductance L_G.

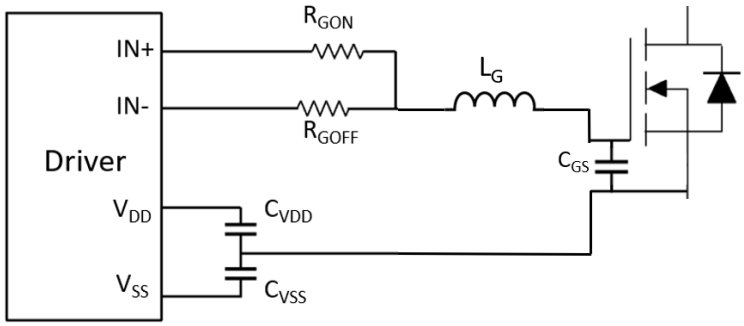


Figure 5 - Gate Loop of SiC MOSFET

L_G is an unwanted parasitic inductance that can resonate with C_{GS} and cause oscillations in the gate-source voltage. These oscillations can lead to ringing in the drain-source voltage. L_G is a lump-sum parasitic inductance which includes package inductance and PCB trace inductance. The PCB trace inductance portion of L_G can be minimized by adhering to the following guidelines:

- Place the driver as close as possible to the SiC MOSFET
- Minimize the gate loop area by having the return path as close as possible to or overlapping with the driver output

Another target for an optimal gate-loop layout is to minimize the overlap between the gate-loop and the power loop. Any overlap between these two loops can lead to an increase in C_{GD} which may result in issues such as higher losses due to parasitic-turn-on.

An example gate-loop layout for a TO263-7 half-bridge circuit is shown in Figure 6. In this recommended layout, components are placed on the top layer, while the return-path plane (SK) is placed on the 2nd layer. By doing this, a smaller driving loop (for both turn-on and turn-off) is formed. This example uses a half-bridge driver to drive both the top and bottom MOSFETs. The placement of this driver and the MOSFETs shows one possible way that the gate-loops of both MOSFETs can both be optimized. In Figure 6, the green arow represents the turn-on gate-driving loop for both top switch and bottom switch.

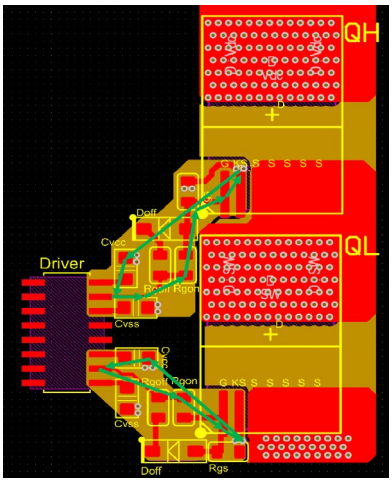


Figure 6 - Driving-loop layout recommendation for the TO263-7 package

The same concept applies to through-hole MOSFETs. In Figure 7, an example of a recommended gate-loop layout is shown for a half-bridge circuit using MOSFETs in TO-247-4 packages. Similar to the above example, the gate driver circuit components are place on the top layer while returning path is on the 2nd layer to minimize the loop inductance.

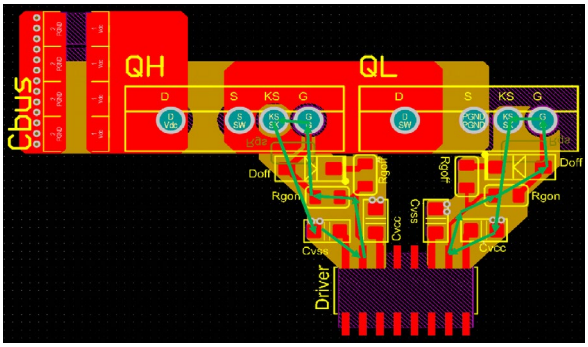


Figure 7 - Driving loop layout recommendation for TO247-4 package

The gate loop inductances were extracted for the TO263-7 example shown in Figure 6 and the results are shown in Table 2.

Table 2 - Extracted gate loop inductances

	Turn-on loop inductance	Turn-off loop inductance
High-side switch	6.8nH	6.6nH
Low-side switch	5.9nH	6.8nH

If we simplify the driving circuit, we can get the equivalent second order circuit shown in Figure 8, where L_G is the parasitic inductance of the gate driving loop, C_{iss} is the input capacitance of the MOSFET and R_g is the gate loop resistance which consists of the internal driving resistance of the MOSFET, the driver internal resistance and the external driving resistor.

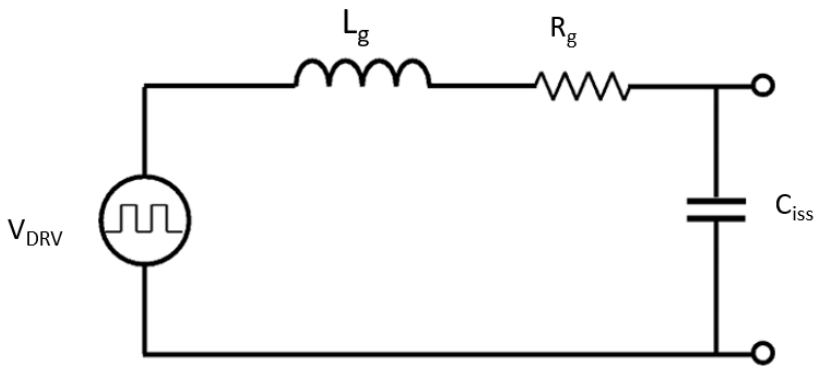


Figure 8 - Equivalent circuit of driving loop

By analyzing this second order circuit, we get the following responses based on the value of R_g:

Underdamped response:

$$R_g < 2 \cdot \sqrt{\frac{L_g}{C_{iss}}}$$

Critically damped response:

$$R_g = 2 \cdot \sqrt{\frac{L_g}{C_{iss}}}$$

Overdamped response:

$$R_g > 2 \cdot \sqrt{\frac{L_g}{C_{iss}}}$$

Using G3R40MT12J in layout shown in Figure 6, the following values are considered:

C_{iss} = 2,897 pF, L_{g_PCB} = 6.8 nH, $L_{g\_Package}$ = 2 nH

It can be calculated that an R_g of 3.5 Ω will give a critically damped response. This means that any R_g greater than or equal to 3.5 Ω will not cause an overshoot in the gate voltage. However, if faster switching is desired, further analysis can be done to optimize the R_g value further.

Figure 9 shows the gate voltage for different values of R_g. It can be determined that an R_g of 3 Ω or 2 Ω can further improve the switching performance while minimizing the gate voltage overshoot and maintaining it below the maximum dynamic gate-source voltage $V_{GS(max)}$ of 22V.

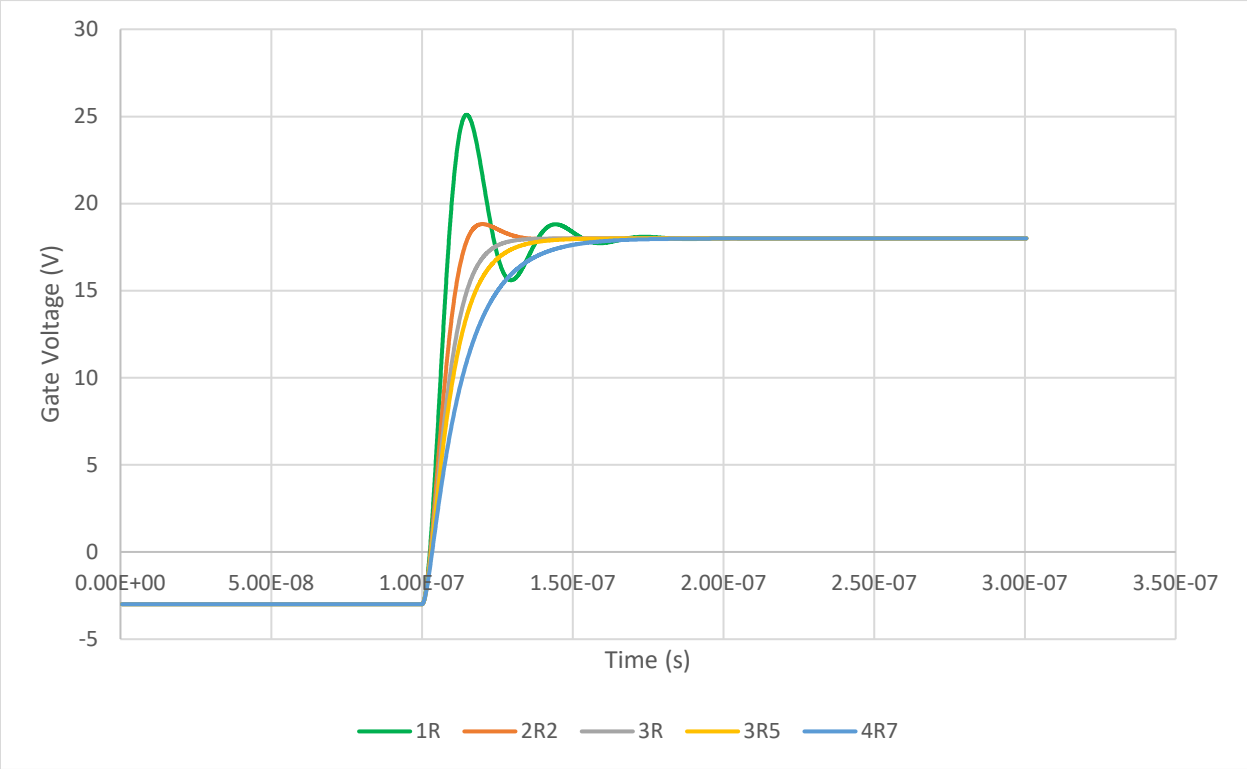


Figure 9 - Step Response for Different R_g Values

The internal gate resistance $R_{g(int)}$ of the G3R40MT12J MOSFET is 1.2 Ω which means that the MOSFET in this example can be driven safely with an external R_{gON} of 0.8 Ω or higher.

4. Power-Loop Layout

The first step in optimizing the power loop layout is to identify the critical high frequency loops. The half-bridge circuit, a common building block for many high-power converters, consists of one high-side device (Q_H), one low-side device (Q_L) and decoupling capacitors (C_{bus}) as shown in Figure 10.

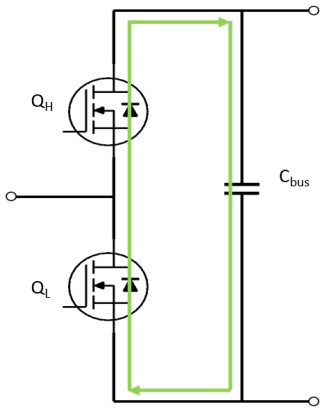


Figure 10 - High Frequency Loop of Half-Bridge Circuit

In this configuration, the high frequency commutation loop (shown in green) is between the high frequency decoupling capacitor and the two switching devices. The parasitic inductance in this loop can cause a higher voltage overshoot at the turn-off transients. The oscillation at turn-off is caused by the resonance between the junction capacitance of the MOSFET and the stray inductance in the power loop. The following guidelines can be followed to minimize the inductance of this loop:

- Place the high frequency decoupling capacitors as close as possible to the MOSFETs
- Use low ESR\ESL multi-layer ceramic capacitors (MLCCs) for C_{bus}
- Reduce the 'high di/dt' loop area on the PCB

For a surface-mount TO263-7 package, one of the recommended layouts is shown in Figure 11. This layout uses inner layer 1 (the closest inner layer to the devices) for the return path of the current, to form a smaller vertical power loop. Since the distance between the PCB's copper layers is very close (only 0.1-0.2 mm), the resulting power loop is very small.

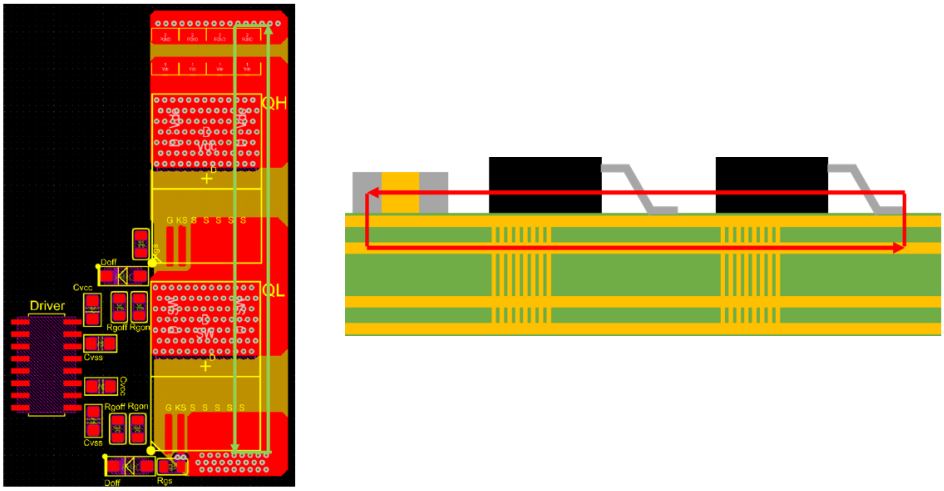


Figure 11 - Vertical High Frequency Loop

Another possible layout is shown in Figure 12. Compared with the previous layout, instead of using a vertical power loop, a horizontal power loop is formed between the two devices and the decoupling capacitors. By putting the decoupling capacitors as close to the device as possible, the power loop can be minimized.

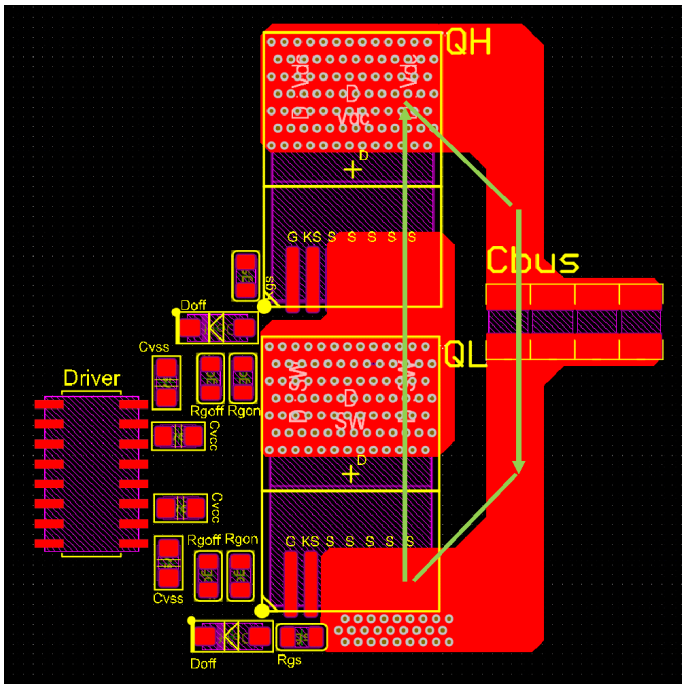


Figure 12 - Horizontal High Frequency Loop

The same concept applies to MOSFETs in a TO247-4 package. A sample example for this package is shown in Figure 13. By using the inner layer that is closest to the device as the return layer, the power loop inductance can be minimized.

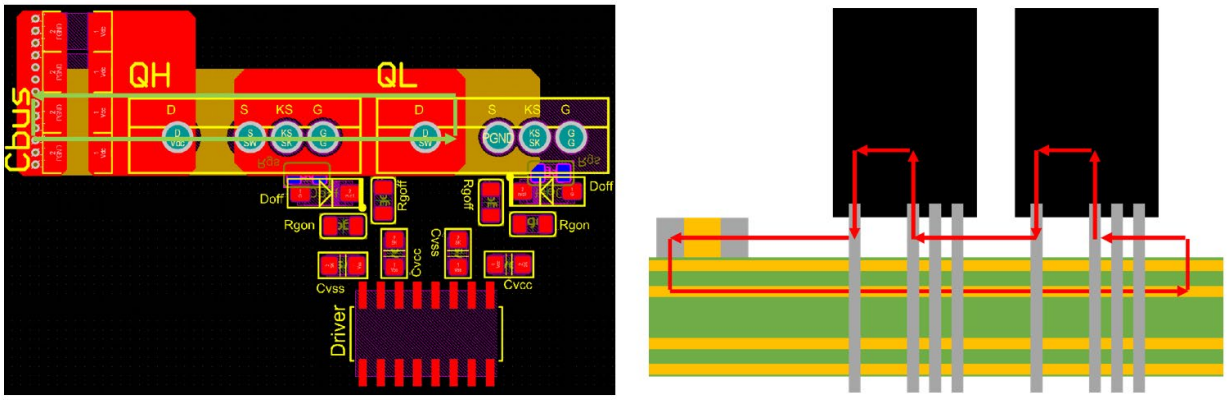


Figure 13 - Recommended power loop layout for MOSFETs in a TO-247-4 package

From Figure 13, it is also clear that with long lead, the loop inductance of the circuit using a TO-247-4 package will be larger than that of the surface mount package (TO-263-7).

3D models have been built (Figure 14) based on the recommended PCB layout and are imported into Ansys Q3D to simulate the loop inductance. The results are summarized in Table 1.

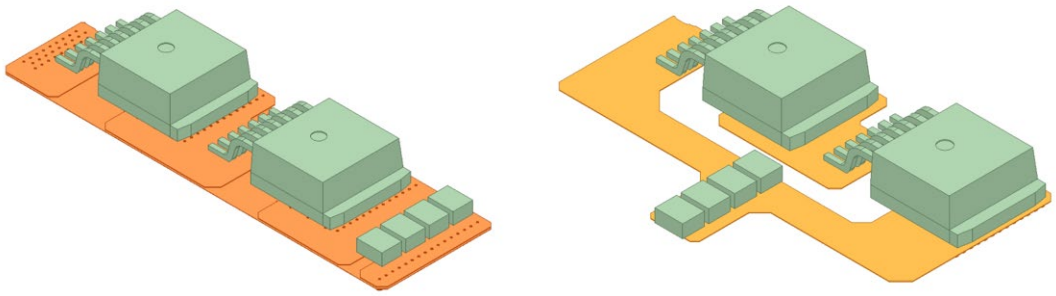


Figure 14 - 3D models for the two PCB layouts used to extract the power loop inductance

Table 3 - Simulated loop inductance for different PCB layout

	Vertical Loop Layout (Figure 11)	Horizontal Loop Layout (Figure 12)
Loop Inductance	5.7nH	19nH

From the simulation results, the vertical loop layout has a smaller loop inductance which results in reduced voltage overshoots.

For device selection, electrical and mechanical models, please refer to https://genesicsemi.com/

Additional Information

Contact: info@navitassemi.com