A Novel Digital Control Strategy for GaN-based Interleaving CrM Totem-pole PFC

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***Abstract*—To meet the high efficiency requirement of data center power supplies, this paper presents a novel digital control strategy focusing on the critical conduction mode (CrM) interleaving totem-pole power factor correction (PFC). A dual-loop and dual-feedforward interleaving control method is proposed, which achieves excellent current sharing, ultra-fast dynamic response as well as small phase error. To achieve full-range zero voltage switching (ZVS) and reduce input current distortion caused by negative current detection delay time, the novel negative inductor current compensation is proposed. Finally, this digital control method is demonstrated on a 500kHz GaN-based interleaving 3.2kW CrM PFC with 99.3% peak efficiency including EMI filter loss.**

Keywords—CrM, totem-pole PFC, digital control, interleaving, negative current, GaN

I. INTRODUCTION

Recently, artificial intelligence and cloud computing technology have developed rapidly, which gives new challenges for data center power supplies in terms of high frequency, high efficiency and high power-density [1]-[2]. With the emergence of gallium nitride (GaN) high electron mobility transistors (HEMTs), GaN based power supply unit (PSU) has been widely researched in various application fields. Furthermore, GaN ICs with integrated drive and protect functions accelerate the application in the industrial filed, which provide high efficiency, huge robust and excellent compatibility with silicon transistors [3]. Therefore, GaN-based totem-pole bridgeless PFC system is widely used in data center power supplies due to fewer components, simple topology structure, low conduction loss and high efficiency.

Conventional GaN-based totem-pole PFC always operates at continuous conduction mode (CCM) with low frequency to acquire low switching loss and high efficiency, but low frequency will increase the volume of magnetic components, which makes it difficult to increase system power density. Soft switching is a good method to enable high efficiency under high frequency. Therefore, the CrM totem-pole PFC becomes popular with zero voltage switching characteristic, which can use smaller inductor by increasing frequency [4]-[6]. However, a disadvantage should be noted for single-phase CrM PFC, the input current ripple is twice of average inductor current, which may result a huge input EMI filter and reduce power density, so as to limit the maximum power level. Thus, multiphase interleaving technology is usually adopted to help reduce input current ripple through ripple cancellation, so as to reduce EMI filter size and improve power level [7]-[10]. Fig.1 shows the two-phase interleaving totem-pole PFC topology, S_1~S_4 are integrated GaN ICs, S_5~S_6 are Si devices, L_A and L_B are the phase inductors, C_o is the output filter capacitor, V_{AC} is the input alternating voltage.

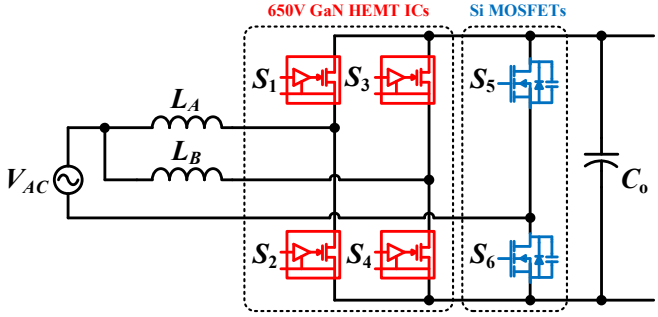


Fig. 1. GaN ICs based two-phase interleaved totem-pole PFC circuit.

For the interleaving CrM totem-pole PFC, there typically have two control strategies: current control mode and voltage control mode. Under the current control mode, peak inductor current is calculated and controlled by close control loop. The turn on signal of main switch is generated by zero current detection (ZCD), and the turn off signal is generated when sampled inductor current is equal to calculated peak inductor current. Since the turn on and turn off signals are generated independently, current control mode has good current balance performance and is insensitive with different inductance between multi phases, and both of the PF and output voltage can be controlled well [11]-[12]. However, the output voltage is needed to directly calculate the peak current reference in this control mode, and the bandwidth of output voltage sampling circuit is ultra-low, so the fast dynamic response is difficult to implement when the load or input voltage change quickly. Under the voltage control mode, the on-time of main switch is decided by single voltage close loop, so it's easy to implement good PF. The on-time is usually constant during a half line cycle, when the load and output voltage are constant. Similar to current

control mode, the sampled output voltage is also needed to directly decide the on-time in voltage control mode, so the dynamic response speed should be slowly [13]-[14]. And it's obvious that the current balance performance under voltage control mode is more sensitive to the different inductance between multi phases, for the on-time is same for different phases, so that this control mode is not suitable for the application of multi-phase CrM PFC.

According to [15], based on current control mode, a dual current control loop hybrid strategy is adopted, which consists two current loops. The outer current loop regulates the average inductor current to the required input current, in order to realize good PF. The inner current loop limits the peak inductor current and valley inductor current through the high speed instantaneous comparison. Due to the addition of outer current loop, the dynamic response can be improved significantly and the current balance performance is not sensitive to the different inductance. But this hybrid control mode adopts triple close loops in total and requires high-speed peak current comparator, which increase the complexity of close control system.

To simplify the control complexity and maintain excellent dynamic response performance, this paper proposes a novel digital dual-loop and dual-feedforward control strategy in Section II. The outer voltage loop is used to regulate the DC output voltage，and the output of the voltage loop is assigned to the multi inner current loops. Every inner current loop regulates the average inductor current, then directly calculate the on-time of main switch, so that the current balance can be realized well. Due to the bandwidth of inner current loop is very high and the feedforward coefficient is added, it's easy to implement fast dynamic response. In Section III, a 500kHz GaN based two phase interleaving 3.2kW CrM totem pole PFC prototype with 99.3% peak efficiency is developed to verify the proposed control strategy.

II. Dual-loop Digital Control Strategy of Interleaved CrM PFC

A. Digital Voltage-Current Dual-loop Control Method

As discussed above, there usually contains two control strategies of voltage-mode and current-mode, and the input current can follow the voltage sinusoidal waveform naturally in traditional CrM PFC rectifiers. Single voltage loop or current loop is enough to meet basic requirements, which can balance voltage stabilization and electrical performance of power factor and iTHD (Total harmonic distortion of input current). But in the GaN-based CrM totem pole PFC, with the switching frequency increasing and the inductor reducing to be a small level, each phase would work with different frequencies due to the tolerance of the inductors which exists in industrial mass production widely. On the one hand, this will lead to poorer phase current imbalance directly. On the other hand, smaller inductor may bring to more significant negative current, which will lead to worser PF and iTHD, terrible EMI, and lower efficiency.

To solve current balance problem and get a fast dynamic response speed in the GaN-based totem-pole PFC, a mixed voltage-current control mode is proposed, which can implement good PF and low THD at the same time. The detailed voltage-current dual-loop and dual feedforward control block diagram is shown in Fig. 2.

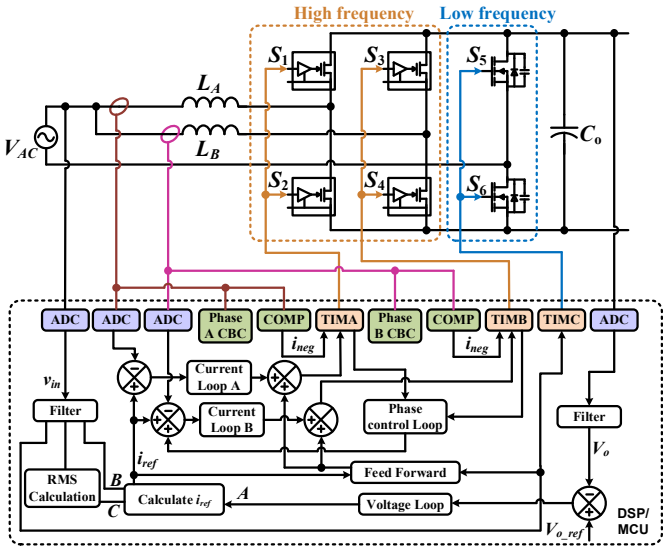


Fig. 2. Interleaving PFC dual-loop and dual feedforward control system.

In this control method, the average inductor current of both phases, output voltage and the input voltage are sampled and filtered by microcontroller. Besides, every single phase control system consists of two control loops based on proportional-integral (PI) controller: the fast inner current control loop and the slower outer voltage control loop. The current control loop is considered to balance the phase currents whose reference value is determined by the voltage loop and phase interleaving control loop. And the feedforward process will determine a theoretical on-time of main switch, which is assigned to the output of current loop. On the control diagram, the current loop's reference i_{ref} can be expressed as:

$$i_{ref} = f(A, B, C) \tag{1}$$

Where A means voltage controller loop output to stabilize output voltage. B is the real time AC input voltage containing sine information whose target is to control the average inductor current to follow input voltage. C is the rms value of AC input voltage. The current loop compares the sampled average current with i_{ref} to generate the on-time of main switch, so that the input current can track input voltage well.

In order to further increase the dynamic performance, an open-loop and theoretical on-time is considered as the feedforward coefficient, which also helps to reduce iTHD additionally. According to the inductor current and input voltage, the coefficient under CrM mode can be derived as:

$$T_{feed\_CrM} = \frac{2L_f \cdot (i_{ref} + i_{neg})}{v_{in}} \tag{2}$$

where i_{neg} is the negative inductor current, it is designed to achieve ZVS during the entire AC cycle. And v_{in} is the real-time input AC voltage, L_f is the inductance of phase inductor.

Although the control system is designed for CrM mode, it may enter discontinuous conduction mode (DCM) when theoretical switching frequency is higher than the given maximum switching frequency. For the average inductor current sample point is set on the half time of main switch on-time usually, the measured current is the true average value during CrM mode, but it's unsatisfied under DCM mode. So the feedforward on-time should be corrected under DCM mode, then the modified feedforward coefficient is:

$$T_{feed\_DCM} = \sqrt{\frac{2L_f \cdot i_{ref} \cdot (v_o - v_{in})}{v_{in} \cdot v_o \cdot f_s}} \quad (3)$$

where f_s is the real switching frequency.

To normalize the feedforward coefficient, those two coefficients will be compared in every calculation cycle and the lower theoretical on-time should be taken. Besides, it's necessary to add a weight coefficient k to adjust the weight of feedforward to meet requirement under different power, which could optimize the control result. Thus, the final feedforward coefficient T_{feed} is derived as:

$$T_{feed} = k \cdot min\left\{\frac{2L_f \cdot (i_{ref} + i_{neg})}{v_{in}}, \sqrt{\frac{2L_f \cdot i_{ref} \cdot (V_o - v_{in})}{v_{in} \cdot V_o \cdot f_s}}\right\} \quad (4)$$

where the k is the adjustable weight coefficient limited between 0 and 1 to optimize the performance of control loop under different operating conditions.

B. Novel Close-loop Control for Phase Interleaving

For high power CrM PFC converter, single phase may bring large input current ripple, which will increase the volume of EMI filter. Multi-phase interleaving CrM PFC can handle high power well and reduce input current ripple by current cancellation, but this will bring a good challenge for the phase interleaving control because the operation frequency is varying within half line cycle even under a constant operating condition. For a given input and load condition, the frequency usually varies three to five times in a half line cycle.

According to the proposed research, the previously different interleaving control methods are divided into two categories of closed-loop and open-loop. Under open-loop control, the turn-on or turn off instant of the slave phase is synchronized with the master phase by delaying half of the switching period of the master, but this control mode is more applied in the low switch frequency situation and it can't guarantee the slave phase working in CrM accurately [16]-[17]. In closed-loop control, phase interleaving is achieved by using the phase error between the two phases as an input of phase control loop and adjusting the on-time of main switch in the slave phase. Therefore, close-loop control is more suitable in high frequency GaN-based CrM PFC for better stability [18].

Based on the above dual-loop control system, a novel phase interleaving close-loop control with another feedforward coefficient is also proposed. The Fig. 3 illustrates the currents and drive signals for interleaving close loop control, in which v_{GS_A} and v_{GS_B} correspond to the main switch's drive signals of each phase respectively, and i_{LA} or i_{LB} is the phase inductor current. To implement phase interleaving, the duration between two adjacent rising edges of v_{GS_A} is marked as T_1, the duration from the rising edge of v_{GS_A} to the next adjacent rising edge of v_{GS_B} is marked as T_2. And T_1 and T_2 are captured by controller repeatedly in each switching cycle. Actually T_1 just indicates the period of master phase A, and T_2 is phase difference between two phases. Ideally if the two phases are interleaved by 180 degrees, the difference of T_1 and T_2 should satisfy $T_2 = T_1/2$ under ideal conditions. With the changing of frequency and other unideal practical conditions, the phase interleaving control loop will eliminate the error between T_2 and $T_1/2$ in real time, so that the phase interleaving can be realized.

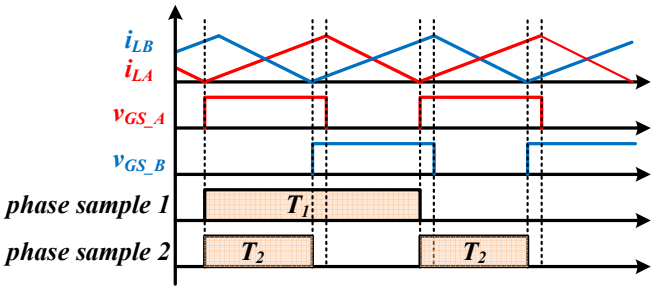
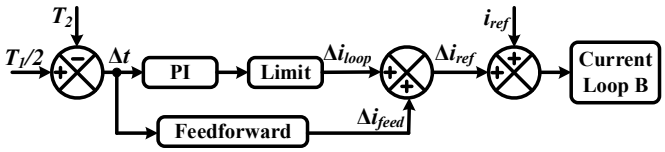
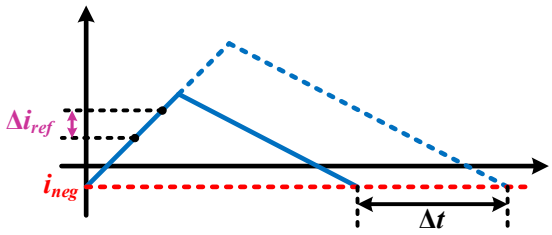


Fig. 3. Typical waveforms of two-phase interleaving operation.

With the above phase information, the control block for phase interleaving loop is depicted in Fig. 4(a), where Δt is calculated through the $T_1/2$ and T_2. In this phase interleaving control method, a PI compensator is adopted to adjust the phase error, so that the phase difference can be maintained to a dynamic equilibrium of around 180-degree interleaving under different conditions. In this phase control strategy, phase B acts as the slave phase whose main switch's on-time is fine-tuned through superimposing the output of phase loop on the inner current loop reference i_{ref} of phase B.



(a)



(b)

Fig. 4. Phase interleaving control strategy. (a) Diagram of the close-loop phase interleaving control. (b) The corresponding between phase error and adjusted current reference value.

As shown in Fig. 4(a), the Δi_{ref} is a combination of Δi_{loop} and Δi_{feed}, where Δi_{feed} is an extra feedforward coefficient,

used to accelerate the interleaving control speed additionally. Based on the theoretical Δi_{feed}, the phase interleaving loop output Δi_{loop} will only be slightly adjusted to deal with the phase error correction. To better explain the feedforward coefficient, the corresponding relation between Δt and Δi_{ref} is figured in Fig. 4(b). After capturing the phase error Δt, the feedforward coefficient can be expressed as following:

$$\Delta i_{feed} = \frac{\Delta t \cdot v_{in}(v_o - v_{in})}{2L_f \cdot v_o} \tag{5}$$

Fig. 5 gives two situations for phase interleaving control. When it needs positive adjustment, a positive Δi_{ref} will be generated, which increases main switch's on-time. As shown in the figure, the positive duration of the green area is longer as the result. On the contrary, a negative Δi_{ref} will decrease on-time of main switch. Combined above adjustment method, phase interleaving can be achieved to meet requirements.

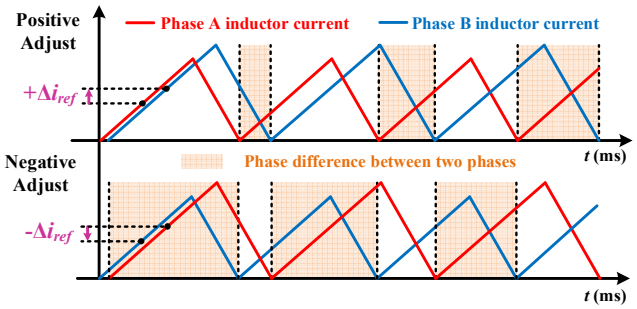


Fig. 5. Positive and negative phase difference adjustment processs.

C. *Full-line-cycle ZVS Control Strategy with ZCD Delay Time Compensation*

For CrM totem pole PFC, achieving full-line-cycle of ZVS is essential to improve efficiency. In traditional CrM converter, ZCD detection circuit is adopted to generate a trigger signal for turning off the SR. However, in practical applications, due to the signal processing delay time introduced from inductor current detection circuit, MCU and gate driver, the instant of SR turning off is later than the actual inductor current crossing zero. Fig. 6 shows the effect of delay time on inductor current.

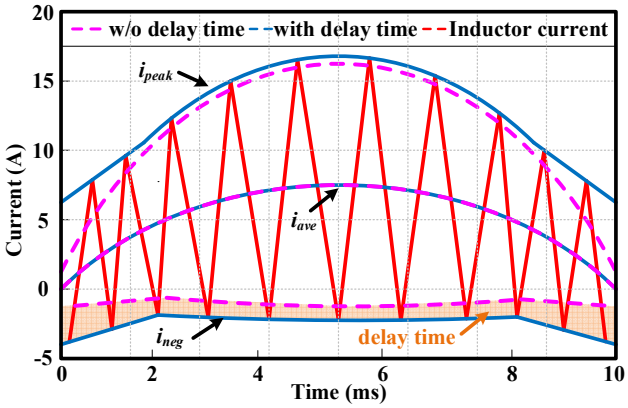


Fig. 6. Comparison of inductor currents between ideal case and the case with delay compensation

As the input voltage decreases, the negative current deviates significantly from the theoretical value, causing the increase of inductor current ripple, leading to the extra conduction loss and worser iTHD. A delay time compensation strategy is analyzed under VOT control, but full compensate is only realized when $v_{in} > 0.5v_o$ [19]. This delay time can also be compensated by detecting the inductor current negative-to-positive ZCD signal, but the strategy requires precision inductor current detection circuit and not suitable for current control mode, especially for high frequency applications [20]. In this paper, a full range ZVS control strategy with full line cycle negative current detection delay compensation is designed based on the above voltage and current dual-loop control system.

To better illustrate the presented ZVS control strategy, the state trajectory of CrM PFC over a switching cycle is given in Fig. 7. When $v_{in} \le 0.5v_o$, $r_2 = v_o - v_{in}$ and $r_2 > v_{in}$, so the main switch can realize soft switching naturally through resonant, during $v_{in} > 0.5v_o$, the v_{ds} can only decrease to $(2v_{in} - v_o)$ if no extra negative inductor current.

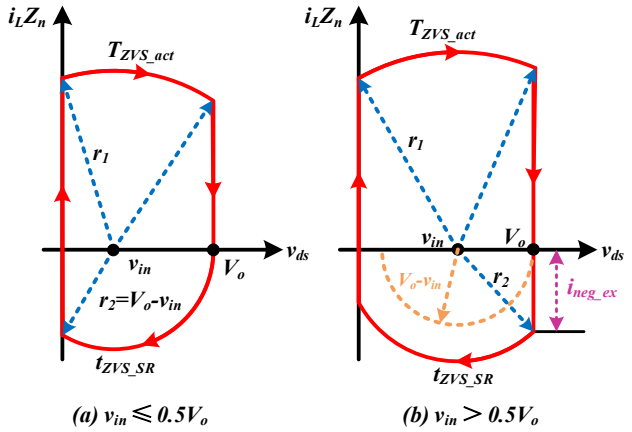


Fig. 7. State plane trajectory. (a) $v_{in} \le 0.5v_o$. (b) $v_{in} > 0.5v_o$.

Thus, a compensation negative current i_{neg} is required to ensure $r_2 \ge v_{in}$ (then ZVS can be achieved). Assuming that GaN devices have consistent parameters and parasitic capacitor $C_{oss1} = C_{oss2} = C_{oss}$, then the i_{neg_ex} that meets the full line ZVS can be expressed as:

$$i_{neg\_ex} \le \begin{cases} 0, & v_{in} \le \frac{V_o}{2} \\ -\sqrt{v_{in}^2 - (V_o - v_{in})^2} \cdot \sqrt{\frac{2 \cdot C_{oss}}{L_f}}, & v_{in} > \frac{V_o}{2} \end{cases} \tag{6}$$

However, there always exists a delay time between negative current detecting signal and SR turn off as mentioned. Negative current detection circuit is shown in Fig. 8, including Hall IC, RC filter, MCU and driver circuit. The whole delay time (T_d) is typically around 100ns, so the negative current will deviate from the theoretical value, which may increase the inductor current ripple and worsen iTHD. Therefore, a full-range ZVS control strategy with negative current detection delay compensation is proposed, which could minimize the inductor current ripple and iTHD, then lowest conduction loss for better efficiency.

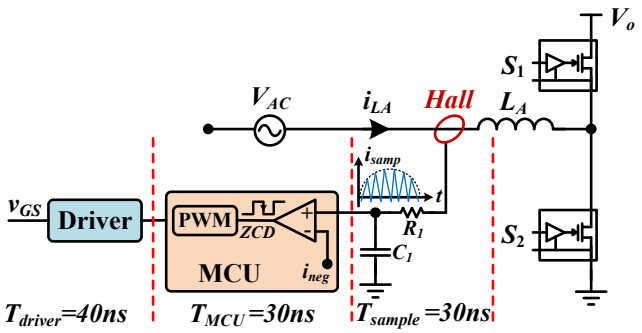


Fig. 8. Negative current detection and driver circuit.

During the processing delay time, an undesired negative inductor current appears for SR keeps on. Since the delay time is not relevant to operating state, the additional negative current change caused by T_d is:

$$\Delta i_{neg} = -\frac{(V_o - v_{in})\cdot T_d}{L_f} \tag{7}$$

Combined with the equations (6) and (7), the compensated extra negative inductor current to achieve full line cycle ZVS can be derived:

$$i_{neg\_ZVS} \le \begin{cases} \frac{(V_o - v_{in})\cdot T_d}{L_f}, & v_{in} \le \frac{V_o}{2} \\ \frac{(V_o - v_{in})\cdot T_d}{L_f} - \sqrt{2V_o v_{in} - V_o^2}\sqrt{\frac{2\cdot C_{oss}}{L_f}}, & v_{in} > \frac{V_o}{2} \end{cases} \tag{8}$$

Another constraint should be noted, with the influence of different load condition, the theory of negative current should be less than the peak inductor current, otherwise the ZCD will not be triggered. Therefore, maximum extra negative inductor current limit is as follow:

$$i_{neg\_ZCD} \le \frac{v_{in}}{L_f}\cdot\sqrt{2\cdot L_f\cdot C_{oss} + t_{on}^2} \tag{9}$$

$$i_{neg} = min\{i_{neg\_ZVS},\ i_{neg\_ZCD}\} \tag{10}$$

Where t_{on} is the real on-time of main switch in every switching cycle, and the i_{neg} will be calculated in every control period.

This compensation strategy can realize full line cycle ZVS and almost full range negative current detection delay time compensation by calculating the theoretical negative inductor current in real time.

III. Experiment Verification

To verify the proposed control strategy, a GaN ICs-based 3.2kW two-phase interleaving digital control CrM totem-pole PFC prototype is built. Table 1 presents the key experiment specifications of the prototype. The switching frequency is limit ed between 50kHz and 500kHz, and a 40μH ferrite inductor is designed for each phase. To implement this novel digital control strategy, a microcontroller STM32G474 is adapted.

For kilowatts power level CrM totem-pole PFC, the peak phase inductor current within a half line cycle may reach to tens of amperes. During the dead time from the turn-off instant of main switch to the turn-on instant of synchronous switch, the large inductor current will flow through the two-dimensional electron gas (2DEG) in GaN device, which will cause a significant dead time loss for the reverse conduction voltage of 2DEG is usually very high. Thus, to achieve higher efficiency, the GaN ICs adapt NV6515 from Navitas' GaNSafe series, which integrated the GaN power transistor, critical protection features as well as driver circuit to enable reliability and robustness. With the integrating technology, the negative drive voltage is not required, so the reverse conduction voltage of 2DEG and dead time loss can be reduced greatly.

TABLE I. KEY PARAMETERS OF PROTOTYPE

Parameter	Value
GaN HEMT IC	NV6515(650V, 35mΩ max)
Si MOSFET	IPT60R022S7
Phase Inductor	40μH
Rated Input Voltage	230VAC
Rated Line frequency	50Hz
Rated Output Voltage	400VDC
Frequency range	50kHz ~ 500kHz

Fig. 9 shows the full load steady-state operation waveforms under 230VAC input and 400VDC output, including input voltage and two-phase inductor currents. The experiment results show that the proposed control method can achieve excellent current sharing performance with current imbalance degree less than 1%. Moreover, 180° phase interleaving is dynamically held well under different input voltage and duty cycle. Besides, negative inductor current distortion can be reduced with detection delay compensation method.

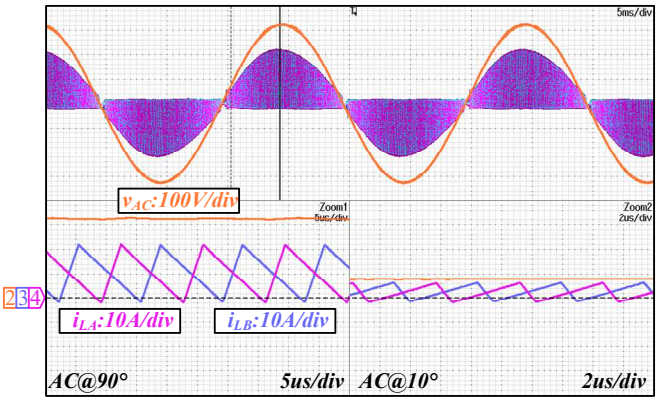


Fig. 9. Full-load operation waveform.

Input dynamic experiment is also tested under AC voltage steps from 180VAC to 264VAC, waveforms are given in Fig.10. Results show that the high bandwidth inner current loop in the novel control strategy can quickly adjust the on-time of main switch within half line cycle to realize the non-sinusoidal envelope inductor current waveform, so as to improve the dynamic response speed and decrease the output voltage adjustment rate.

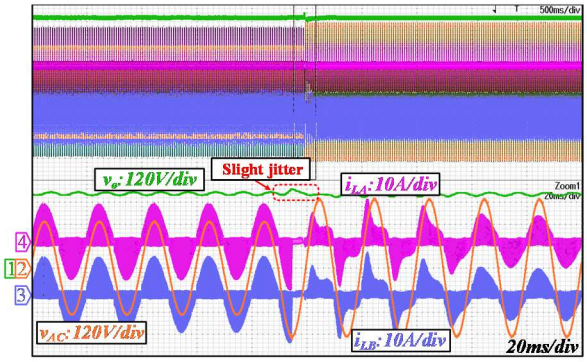


Fig. 10. AC input voltage step from 180VAC to 264VAC.

Fig.11 presents the efficiency curve including the loss of EMI filter and power stage. The peak efficiency of the prototype can reach 99.3%.

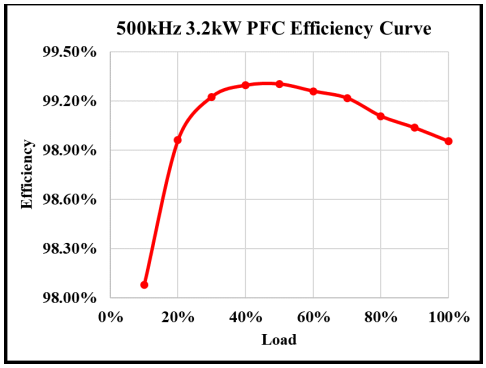


Fig. 11. Measured efficiency of 3.2kW prototype.

IV. Conclusions

This paper proposed a novel digital control method for GaN-based CrM totem-pole PFC. Compared to conventional current control mode or voltage control mode, this dual-loop digital control system achieves high precision current sharing, well phase interleaving performance and fast dynamic response. Furthermore, full-range ZVS and negative current detection delay compensation is implemented. Finally, the proposed control strategy is verified by the experimental results of a 500kHz 3.2kW GaN-based interleaving CrM totem-pole PFC prototype with an outstanding peak efficiency of 99.3%.

References

[1] C. Song and H. Li, "Evaluation of Efficiency and Power Factor in 3-kW GaN-Based CCM/CRM Totem-Pole PFC Converters for Data Center Application," 2023 11th International Conference on Power Electronics and ECCE Asia, Jeju Island, Korea, Republic of, 2023, pp. 2663-2668.

[2] J. -Y. Lee, J. -H. Chen and K. -Y. Lo, "Design of a GaN Totem-Pole PFC Converter Using DC-Link Voltage Control Strategy for Data Center Applications," in IEEE Access, vol. 10, pp. 50278-50287, 2022.

[3] B. Li, X. Huang, J. Zhang, T. Wei and J. Zhu, "High-Frequency High-Efficiency LLC Module with Planar Matrix Transformer for CRPS Application Using GaN Power IC," International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), Nuremberg, Germany, 2023, pp. 1-7.

[4] J. Li, Z. Chen, S. Zhang and X. Wu, "Implementation of Close-Loop Control for Interleaved CrM Totem-Pole PFC Converters with GaN Devices," 2023 IEEE 14th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Shanghai, China, 2023, pp. 137-140.

[5] Y. Liu, X. Wu and S. Zhang, "A Simple Input Filter Capacitance (IFC) Current Compensation Scheme for CRM Totem-Pole PFC With Si MOSFETs at 800 Hz Line Frequency," in IEEE Transactions on Industrial Electronics, vol. 71, no. 8, pp. 9405-9416, Aug. 2024.

[6] J. Sun, X. Huang, N. N. Strain, D. J. Costinett and L. M. Tolbert, "Inductor Design and ZVS Control for a GaN-Based High Efficiency CRM Totem-Pole PFC Converter," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 727-733.

[7] Q. Ma, Q. Huang, R. Yu, T. Chen and A. Q. Huang, "Digital Interleaving Control for Two-Phase TCM GaN Totem-Pole PFC to Reduce Current Distortion," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 3682-3688.

[8] J. Zhang, L. Li and X. Zhang, "Hybrid Modulation Interleaving Scheme for CRM Totem-Pole Bridgeless PFC Rectifier," 2020 15th IEEE Conference on Industrial Electronics and Applications (ICIEA), Kristiansand, Norway, 2020, pp. 805-810.

[9] Q. Huang and A. Q. Huang, "Review of GaN totem-pole bridgeless PFC," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 3, pp. 187-196, Sept. 2017.

[10] Z. Liu, Z. Huang, F. C. Lee and Q. Li, "Digital-Based Interleaving Control for GaN-Based MHz CRM Totem-Pole PFC," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 808-814, Sept. 2016.

[11] M. Torrisi and S. Messina, "Three-Channel Interleaved Totem Pole PFC in Triangular Current Mode (TCM) with STM32G474 Microcontroller," International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), Online, 2021, pp. 1-6.

[12] Q. Huang, R. Yu, Q. Ma and A. Q. Huang, "Predictive ZVS Control With Improved ZVS Time Margin and Limited Variable Frequency Range for a 99% Efficient, 130-W/in3 MHz GaN Totem-Pole PFC Rectifier," in IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 7079-7091, July 2019.

[13] Y. Liu, X. Huang, Y. Dou, M. Li, O. Ziwei and M. A. E. Andersen, "Adaptive dead time control for ZVS GaN based CRM Totem Pole PFC," 2020 IEEE 9th International Power Electronics and Motion Control Conference (ECCE Asia), Nanjing, China, 2020, pp. 438-442.

[14] C. Marxgut, F. Krismer, D. Bortis and J. W. Kolar, "Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier," in IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 873-882, Feb. 2014.

[15] Q. Huang, R. Yu, A. Q. Huang and W. Yu, "Adaptive zero-voltage-switching control and hybrid current control for high efficiency GaN-based MHz Totem-pole PFC rectifier," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 2017, pp. 1763-1770.

[16] Q. Ma, Q. Huang, R. Yu, T. Chen and A. Q. Huang, "Digital Interleaving Control for Two-Phase TCM GaN Totem-Pole PFC to Reduce Current Distortion," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 3682-3688.

[17] Z. Liu, Z. Huang, F. C. Lee and Q. Li, "Digital-Based Interleaving Control for GaN-Based MHz CRM Totem-Pole PFC," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 808-814, Sept. 2016.

[18] J. Li, Z. Chen, S. Zhang and X. Wu, "Implementation of Close-Loop Control for Interleaved CrM Totem-Pole PFC Converters with GaN Devices," 2023 IEEE 14th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Shanghai, China, 2023, pp. 137-140.

[19] Y. Yang et al., "SR Control With Zero Current Detection Delay Compensation for GaN CRM Totem-Pole PFC Rectifier," in IEEE Transactions on Power Electronics, vol. 38, no. 6, pp. 7059-7068, June 2023.

[20] Z. Huang, Z. Liu, Q. Li and F. C. Lee, "Microcontroller-based MHz totem-pole PFC with critical mode control," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 2016, pp. 1-8.