NVE107C - User Guide: 650V Bi-directional GaN Eval Board

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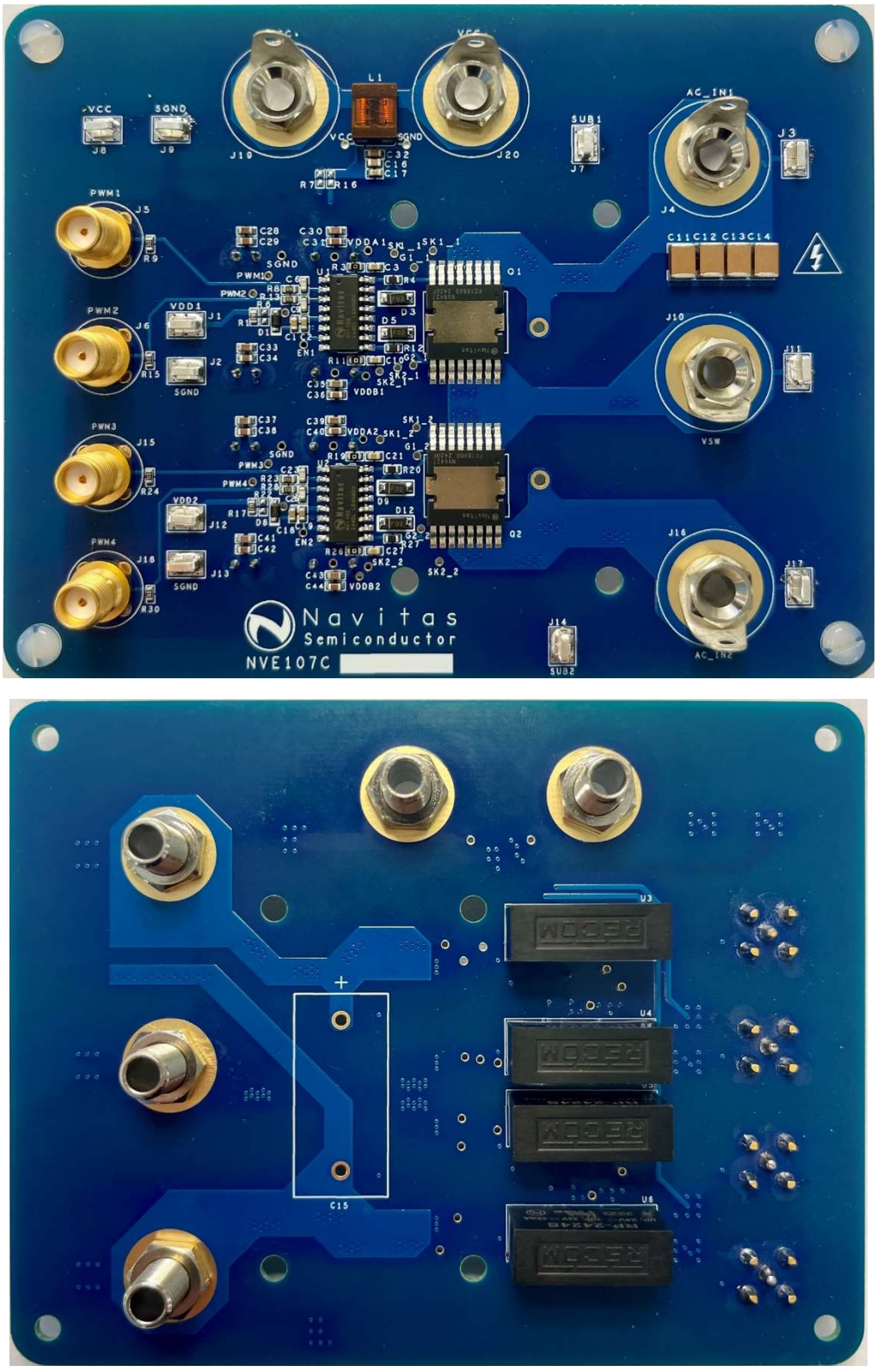

Figure 1 – Top side and bottom side of the NVE107C eval board

1. Features

The NVE107C evaluation board (Figure 1) consists of a power stage using two bi-directional GaN switches (NV6427) in a half-bridge configuration. The bi-directional switches are driven by Navitas' NV1702 IsoFast™ isolated dual-channel GaN driver.

NV6427 is an optimized bi-directional switch capable of blocking voltage in both directions. The advantages of a bi-directional switch over the traditional two series connected switches are:

1. Potentially four times reduction in the active chip area
2. Two to Four times reduction in the PCB footprint area
3. 20x Qg and 10x output capacitance reduction compared to series connected Si switches

The power density benefit of using a bi-directional switch can be visualized in Figure 2 below.

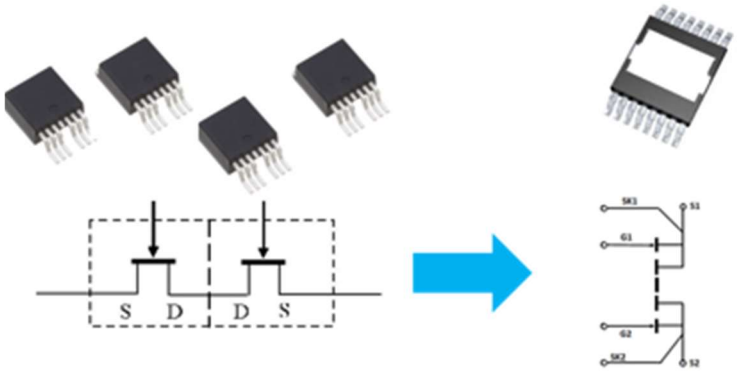

Figure 2 - Series connected switch vs. bi-directional switch solution

1.1. Substrate Management of Bi-directional GaN Switch

Substrate management is crucial for the proper functioning of a bi-directional GaN switch. A floating substrate can result in large Rdson drift and possibly early device saturation (Figure 3). This can lead to excess power loss, elevated device temperatures and possibly system failure.

Navitas' bi-directional GaN switches include a monolithic, integrated substrate management circuit which automatically connects substrate to the lowest source terminal voltage. Navitas' unique substrate management technology allows optimized switching performance during four-quadrant operation (Figure 3).

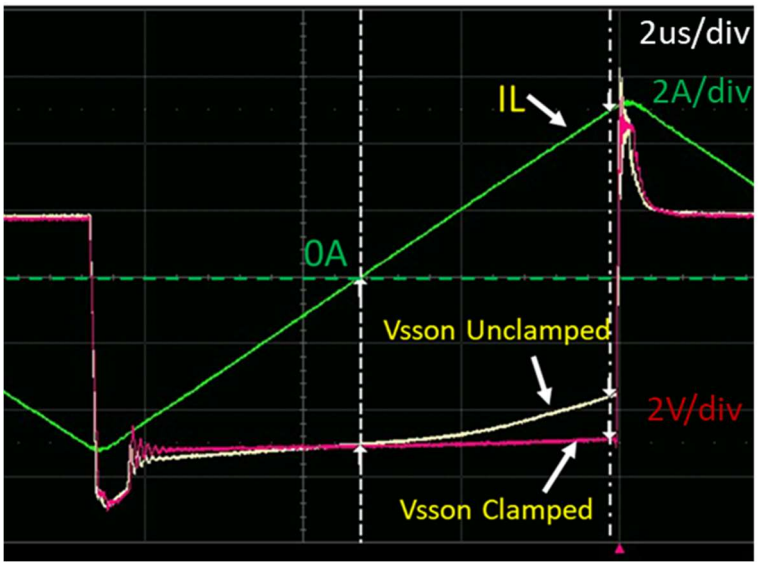

Figure 3 - Early saturation of bi-directional switch with unclamped substrate compared to the superior performance of a switch with a clamped substrate

Navitas's active clamp technology also outperforms the alternative approach of passive diode clamp. (Figure 4).

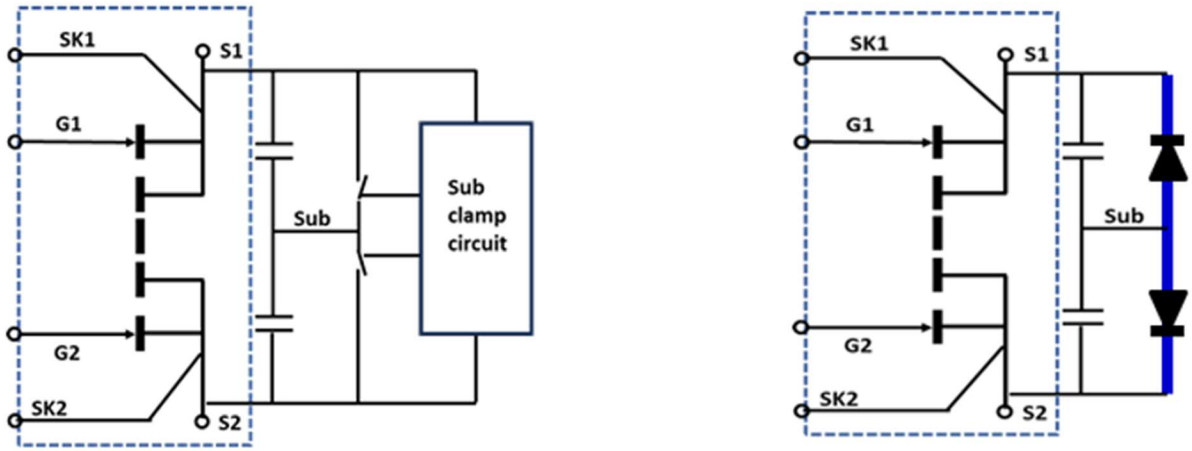

Figure 4 - Navitas's active clamp technology (left). Passive diode clamp method (right)

In a switching test (Figure 5), the performance of these two methods were compared.

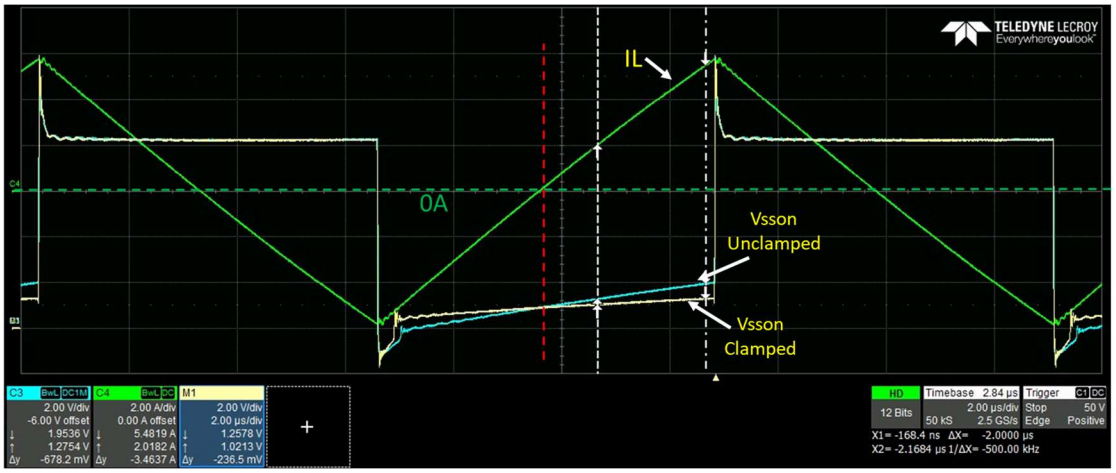

Figure 5 - Comparing Navitas's active substrate clamping to passive diode clamping method

During this test, Navitas' bi-directional switch (yellow waveform) outperformed a similarly rated bi-directional switch (blue waveform) which was using the diode substrate clamp solution. The device temperatures and on-state resistance values were measured during the test and are summarized in the table below.

	On-state resistance	Case Temperature
Navitas with integrated substrate clamp	68mΩ	61℃
Substrate with diode clamp	196mΩ	76℃

It is important to note that the high on-state resistance of the passive clamp solution is due to the back-gating effect of improper substrate management.

1.2. NV1702 Gate Driver IC

The NV1702 IC is a dual-independent-channel isolated GaN driver. This device has two fully isolated drivers specifically designed to drive GaN power switches with medium on-resistance and low dV/dt applications (10V/ns to 30V/ns). The digital input controls are galvanically isolated from the drivers' sides. It provides isolation above 10 kV surge voltage and can sustain common mode transients as large as 200V/ns. The secondary side of the NV1702 IC accepts a wide range of supply voltages (9V to 19.8V) and can drive the bi-directional switch with an internally regulated gate voltage of 6.2V nominal. This feature eliminates the need to provide a dedicated regulated voltage rail for the gate driver. The NV1702 driver IC is also compatible with bootstrap solutions.

The NV1702 is optimized for switching applications. It comes equipped with a blanking feature making it robust against input noise induced by hard-switching events. The IC also consumes very low quiescent current (350μA on input supply and 390μA on each output supply) making it an ideal choice for high efficiency applications.

The NV1702 driver features optimized output impedance, ensuring compatibility with Navitas' bi-directional switches and enabling a straightforward unipolar gate drive scheme (0V to 6.2V). This eliminates the need for a negative voltage rail, which is required with a traditional GaN discrete driver.

1.3. Slew Rate (dV/dt) Control

The NV1702 driver can typically source 80mA and sink 300mA of current which is sufficient to drive a medium family of bi-directional switches. A typical gate drive circuit is illustrated in Figure 6 below.

A resistor is placed between the outputs of the NV1702 driver and the gates of the bi-directional switches to control the turn-on slew-rate. NVE107C comes populated with 4.99Ω gate resistors (R4 and R12 in Figure 6) to control the turn-on slew-rate of the NV6427 devices. Depending on the test circuit and testing conditions, these gate resistors can be modified to tune the slew-rate to the desired range.

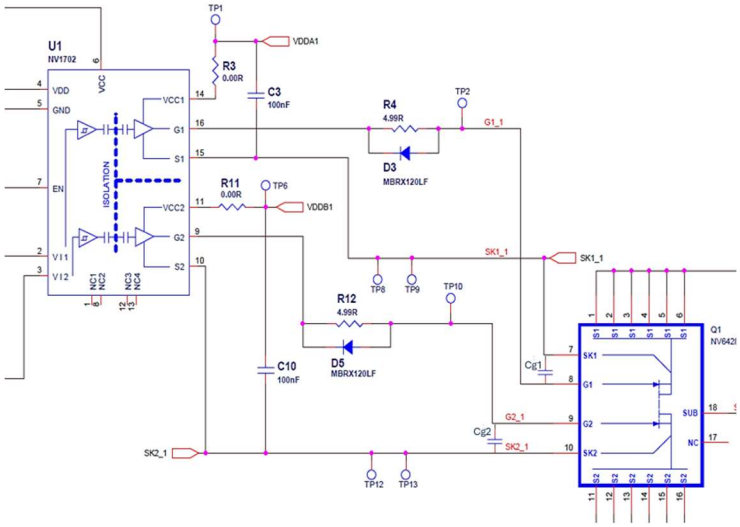

Figure 6 - Gate drive circuit

Diodes are connected in parallel to the gate resistors to provide a lower impedance path for turn-off. These are illustrated by D3 and D5 in Figure 6. This lower impedance path also provides increased dV/dt immunity to combat against unwanted turn-on induced by external dV/dt events. Therefore, to tune the turn-off slew-rate while maintaining this lower impedance path, it is recommended to use capacitors connected between the gate and kelvin source pins on the bidirectional switch. These capacitors are illustrated by Cg1 and Cg2 in Figure 6. It is recommended to use external gate capacitors of 1nF for optimal operation of the NV1702 gate driver IC with the NV6427 bi-directional switch. For NV6428, this capacitor is not needed due to larger gate charge.

Since the external gate capacitors will form an RC network with the gate resistors, these capacitors will also impact the turn-on slew-rate. Therefore, if these capacitors are modified, it might be necessary to re-tune the gate drive resistors.

2. Board Connections

The electrical connections of the NVE107C eval board are shown in Figure 7.

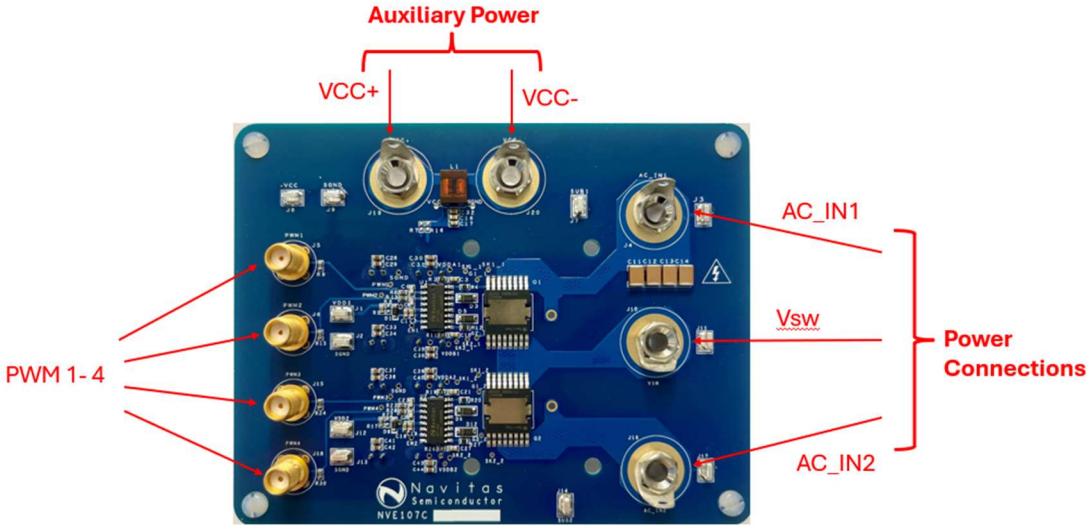

Figure 7 - Board Connection Points

The board operates with a nominal 12V auxiliary voltage supply, which powers four on-board isolated power supplies and the primary side of the two NV1702 isolated GaN drivers.

Each isolated power supply features a 1:1 turns ratio, resulting in four isolated 12V rails on the secondary sides of the NV1702 ICs. The NV1702 then internally regulates this voltage to deliver a nominal 6.2V gate drive for the bi-directional switches.

3. Example Test Circuits

The NVE107C test board provides significant flexibility, allowing for the implementation of various test circuits based on the PWM sequencing and power connections.

The versatility of the bi-directional switch allows it to be used in several applications such as in AC/AC matrix inverters, on-board chargers and solar inverters (Figure 8).

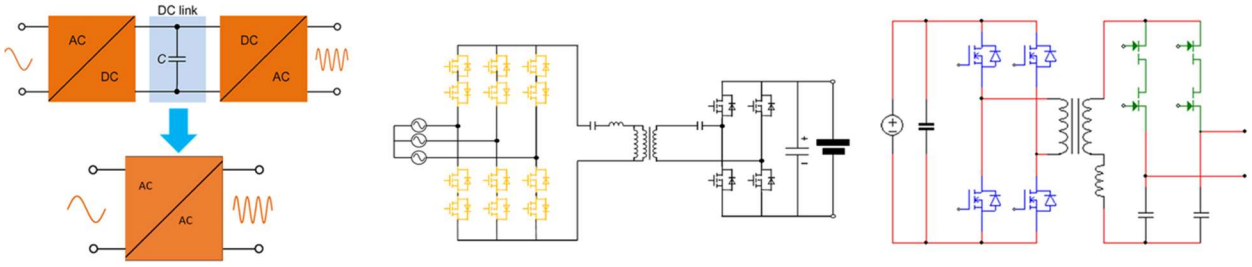

Figure 8 - Applications of bidirectional switch. AC/AC matrix inverters (left), on-board chargers (middle) and solar micro-inverters (right)

The sections below demonstrate a few examples of test circuits using the NVE107C demo board.

3.1 Clamped Inductive Switching

In the clamped inductive switching configuration, the inductor current builds up during each switching cycle. To prevent excessive current, PWM signals should not be generated continuously; instead, burst mode operation should be used to limit the number of applied cycles during testing.

This test configuration is particularly useful for evaluating circuit performance at higher currents without requiring a thermal management solution. The short pulse durations minimize power dissipation, reducing thermal stress on the system.

A simplified block diagram for this test is shown in Figure 9:

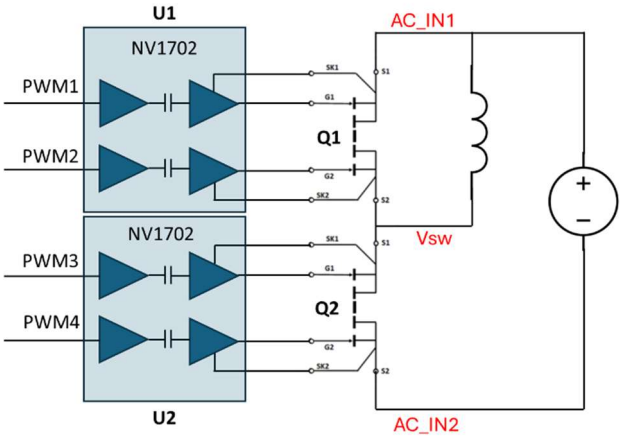

Figure 9 - Clamped Inductive Switching Test Circuit

It is important to note that in this test configuration, Q2 serves as the active device, with the inductor connected in parallel to Q1. Since Q1 and Q2 are bi-directional switches capable of blocking current in both directions, precise PWM sequencing is crucial to ensure proper current flow. For example, the PWM sequencing for the test circuit shown in Figure 10 is shown below. PWM1 and PWM3 for this example are biased as dc high.

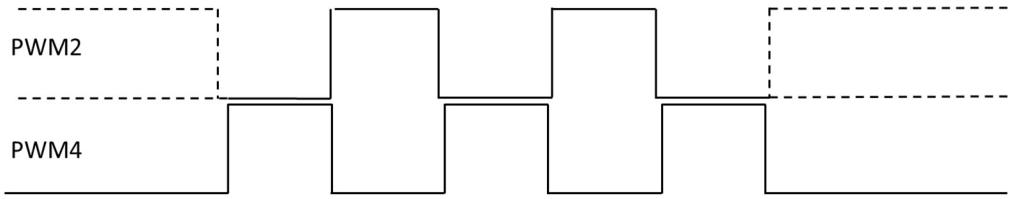

Figure 10 - PWM sequence for the Clamped Inductive Switching test

The dotted lines for PWM2 indicate that its logic state can be either high or low before the first active pulse of PWM4 begins. During the burst pulse sequence, PWM2 operates synchronously with PWM4 to minimize losses in the freewheeling device, Q1.

The PWM sequence illustrated above represents a burst of three pulses, but this logic can be extended to any number of pulses (N), provided that the safe operating area (SOA) limits of the active devices and the saturation current of the inductor are not exceeded. Example waveforms for this test are shown below in Figure 11.

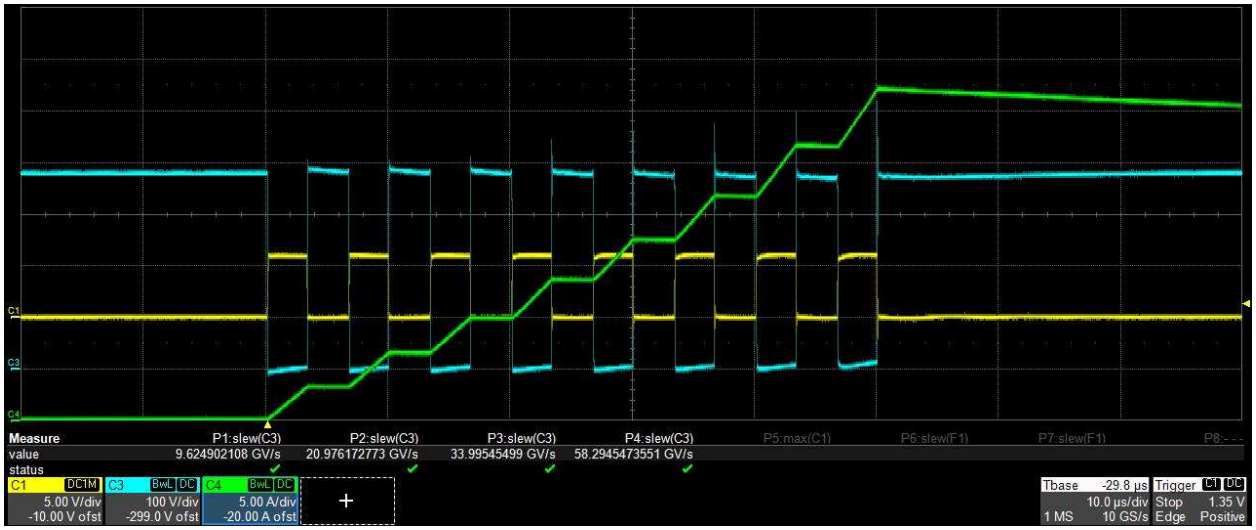

Figure 11 - Clamped Inductive Switching Waveforms

In this test, 8 bust pulses are applied to the test circuit. Channel 1 shows the gate waveform G2 for the active device Q2. Channel 3 is the voltage across Q2 measured with a differential probe (from Vsw to AC_IN2). Channel 4 shows the inductor current. During this burst, the inductor current builds up to a peak of 32A. This test was done while maintaining the temperature of the NV6428 bi-directional switches and the NV1702 ICs at 125C demonstrating the robustness of the system under thermal stress. NV6427 is a higher Rdson device and will handle half of the peak switching current shown above.

3.2 AC/AC

An AC/AC inverter can be implemented using the NVE107C demo board by configuring it as follows (Figure 12):

- An external LC network can be connected from Vsw to AC_IN2
- An external load can be connected in parallel to Cout

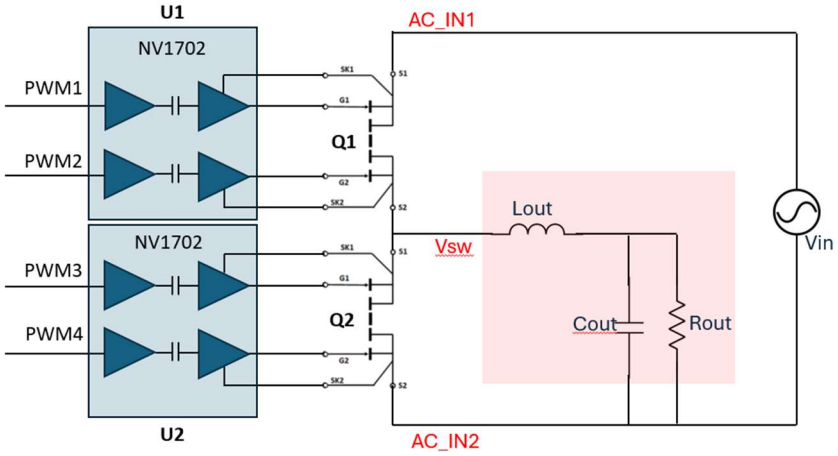

Figure 12 - Implementation of AC/AC inverter using the NVE107C demo board

The PWM signals must be synchronized to the AC input waveform and can be generated externally using analog circuitry or a microcontroller.

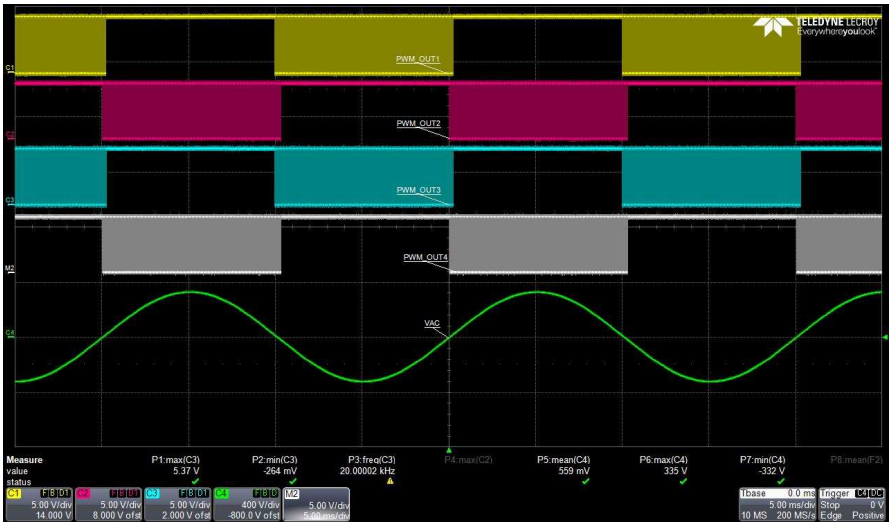

Figure 13 - PWM sequence for AC/AC operation

Figure 13 shows the PWM sequencing relative to the input AC voltage.

This inverter which operated under the zero voltage switching condition was ran at 230Vac, 500kHz switching, and 500W load. No heatsink was used to cool the NV6427 ICs; a fan solution was sufficient for this test. The thermal image of this inverter running at 500W is shown below.

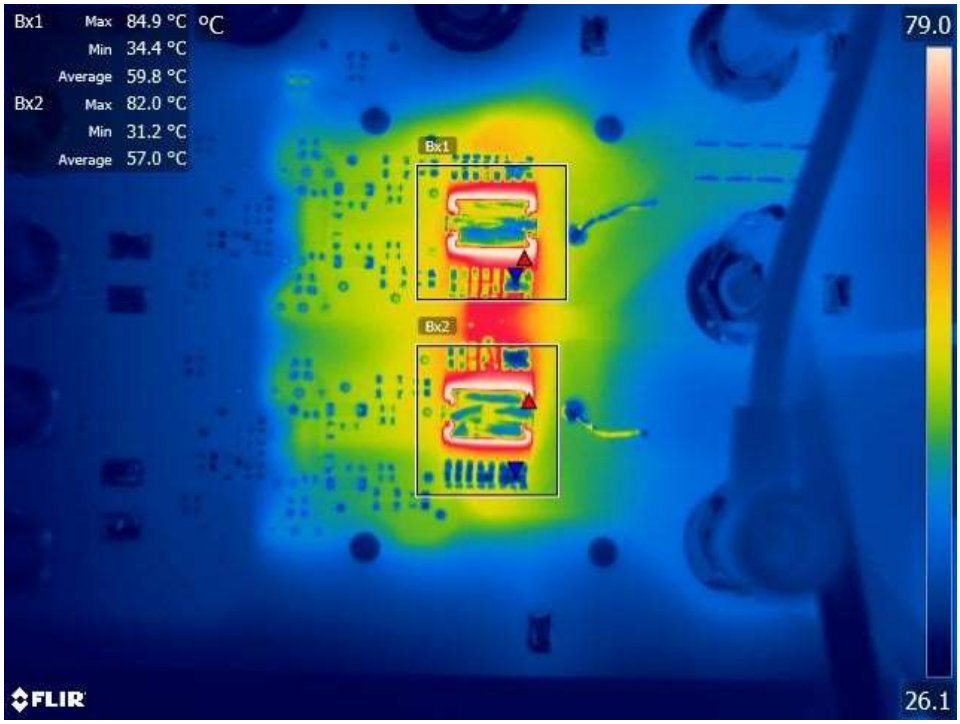

Figure 14 - Thermal image of 500W AC/AC inverter running at 230Vac and 500W

This test shows that the case temperature of the devices was maintained below 85℃ demonstrating low losses and effective substrate management of the bidirectional switches.

Bi-directional GaN switch is configured in TOLT, which is a top cooled package. **Even though it is efficient, it is recommended to use air flow or add a heatsink during evaluation**. TOLT won't be able to transfer power dissipation into PCB or ambient without air flow or a heatsink

4. Schematic

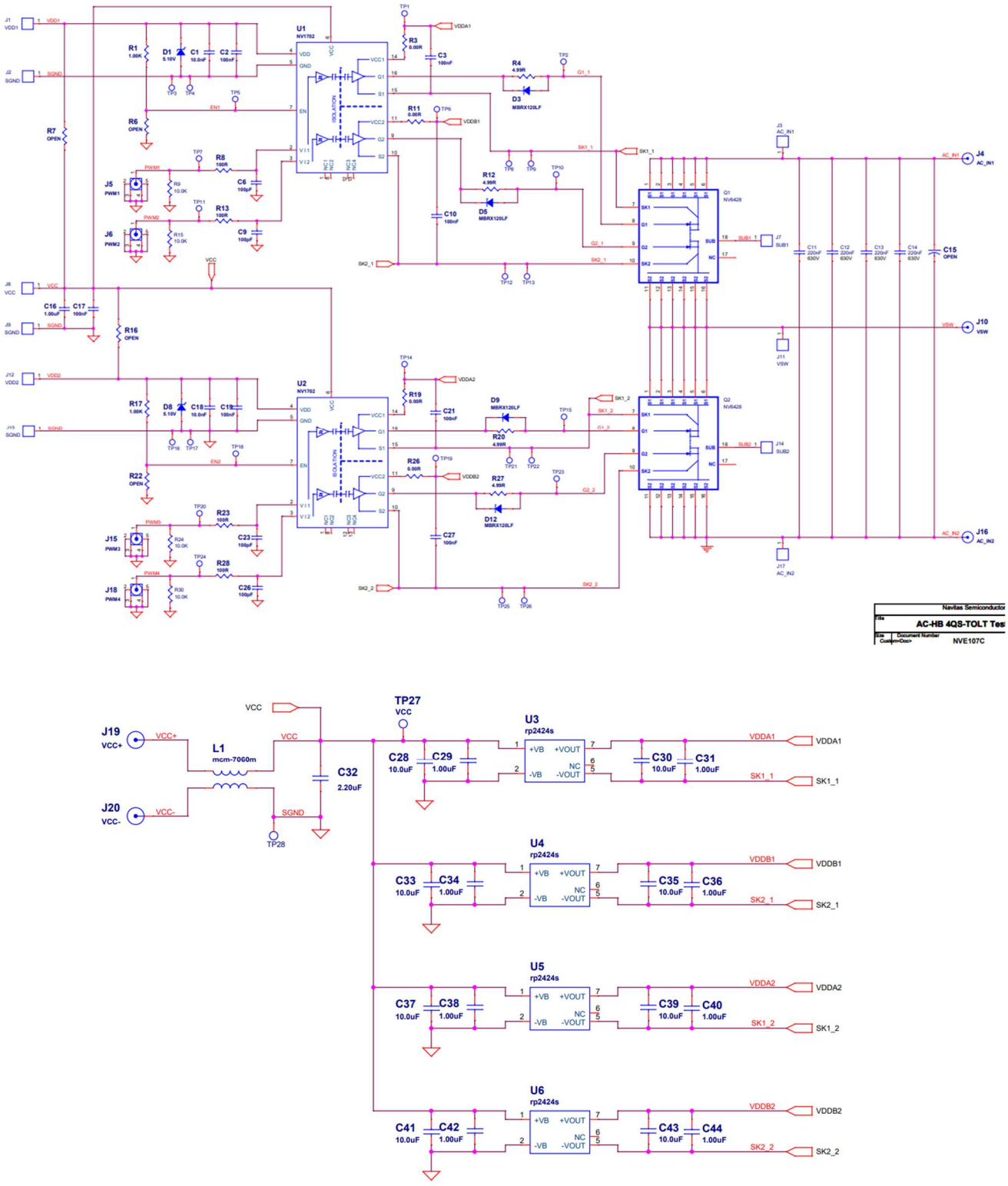

Figure 15 - Schematic of the NV107C eval board

5. PCB Layout

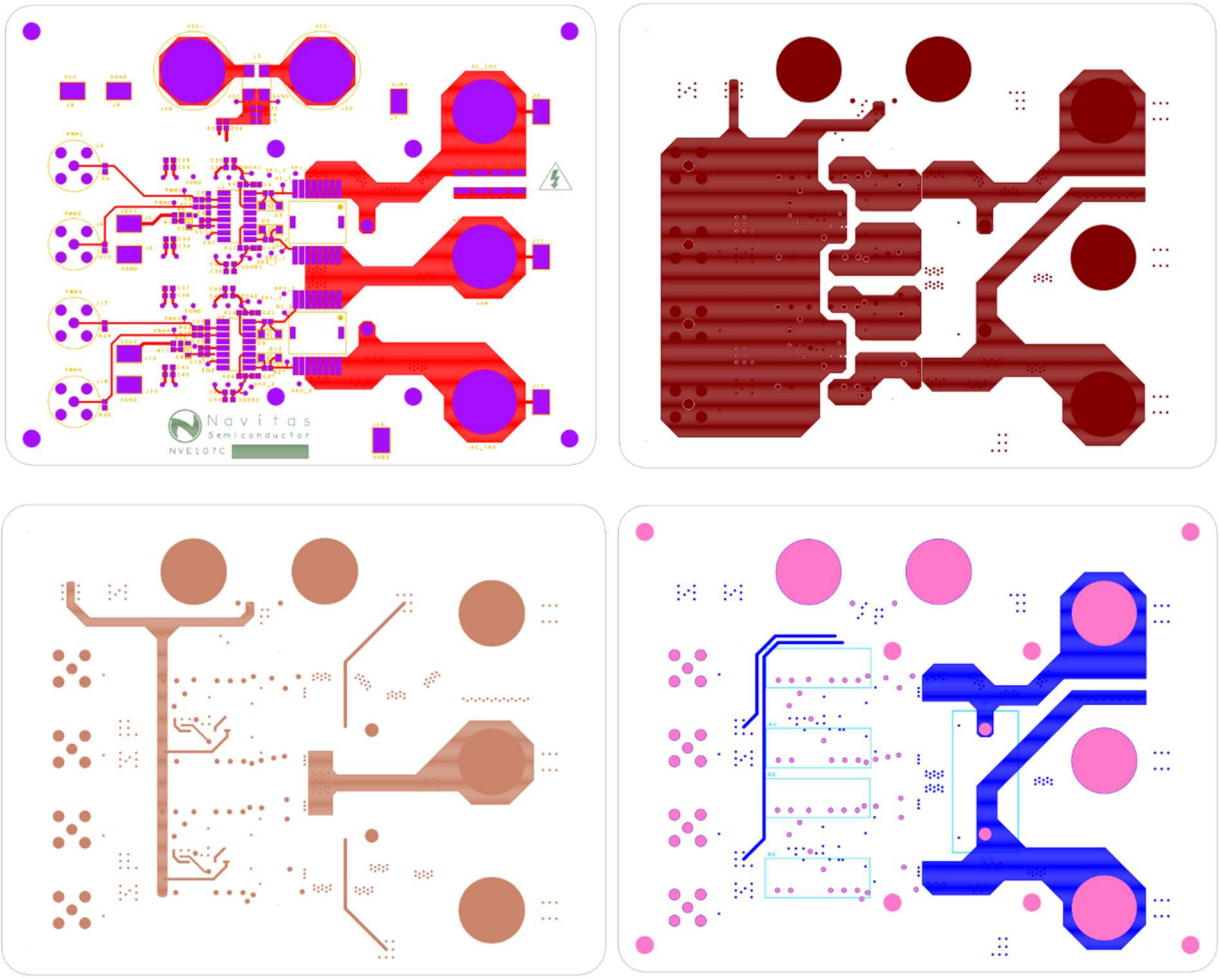

Figure 16 – Layout of the NV170C PCB. Top left is the top layer. Top right is mid layer 1. Bottom left is mid layer 2. Bottom right is the bottom layer.

6. Bill of Material

REFERENCE	DESCRIPTION	MFGR. NAME	MFGR. PART #
C1, C18	CAP CER 10000PF 50V 10% X7R 0603	AVX Corporation	06035C103KAT2A
C10, C17, C19, C2, C21, C27, C3	CAP CER 0.1uF 50V X7R 0603	Kemet	C0603C104M5RACTU
C11, C12, C13, C14	CAP CER 0.22UF 630V X7T 1812	TDK Corporation	C4532X7T2J224K200KC
C16	1µF ±10% 50V Ceramic Capacitor X7R 0603	Taiyo Yuden	UMK107AB7105KA-T
C23, C26, C6, C9	CAP CER 100PF 25V C0G/NP0 0603	Kemet	C0603C101J3GACTU
C28, C30, C33, C35, C37, C39, C41, C43	CAP CER 10UF 35V X5R 0603	Murata Electronics	GRM188R6YA106MA73D
C29, C31, C34, C36, C38, C40, C42, C44	CAP CER 1uF 35V X5R 0603	Samsung Electronic	CL10A105KL8NNNC
C32	2.2µF ±10% 25V Ceramic Capacitor X6S 0603	Murata Electronics	GRT188C81E225KE13D
D1, D8	DIODE ZENER 5.1V 200MW SOD323F	ON Semiconductor	MM3Z5V1B
D12, D3, D5, D9	DIODE SCHOTTKY 20V 1A SOD123	Micro Commercial	MBRX120LF-TP
J1, J11, J12, J13, J14, J17, J2, J3, J7, J8, J9	PC TEST POINT COMPACT SMT	Keystone Electronics	5016
J10, J16, J19, J20, J4	Banana Jack	Johnson Components	108-0740-001
J15, J18, J5, J6	RF Connectors PCB straight jack 50ohm	Emerson Connectivity	142-0701-201
L1	CMC 1A 2LN 2.7KOHM SMD	Mag Layers	MCM-7060M-272-RU
Q1, Q2	Navitas GaN Fet	Navitas	NV6428
R1, R17	RES 1K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1001V
R11, R19, R26, R3	Thick Film Resistors - SMD 0603 Zero Ohms	Panasonic	ERJ-3GEY0R00V
R12, R20, R27, R4	RES SMD 4.99 OHM 1% 1/10W 0603	Vishay	CRCW06034R99FKEA
R13, R23, R28, R8	Thick Film Resistors - SMD 0603 100ohms 1% Tol	Panasonic	ERJ-3EKF1000V
R15, R24, R30, R9	RES 10K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1002V
R16, R22, R6, R7, TP1, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP2, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP3, TP4, TP5, TP6, TP7, TP8, TP9	Open component	-	-
U1, U2	Dual independent channels digital isolator	Navitas	NV1702
C15	Open component	-	-
U3, U4, U5, U6	DC DC CONVERTER 24V 1W	Recom Power	RP-2424S

IMPORTANT NOTICE:

Hazardous voltages are present on this demo board. Personal contact with high voltages may result in injury or death. Correct handling and safety procedures must be observed. Boards are for lab bench evaluation only. Not for installation in end-user equipment.

CAUTION:

This board contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

Additional Information

Contact: info@navitassemi.com