Redefining Data Center Power: GaN and SiC Technologies for Next-Gen 800 VDC Infrastructure

Artificial Intelligence (AI) Is Fueling Data Center Demand

The rapid development and deployment of massive artificial intelligence (AI) in the cloud, including OpenAI's ChatGPT, is drawing new and more powerful, purpose-designed AI processors into data center servers. AI, which encompasses machine learning (ML), deep learning (DL), and generative AI, mimics human-like tasks, behaviors, and intelligence and is altering the way sectors such as automotive, manufacturing, and healthcare conduct business.

To cope with demand, the number of data centers deployed globally has doubled in the last decade, to 7,000. By 2026, data centers globally are expected to consume 1,000 TWh, more than double the 2022 figure (460 TWh) and a level that the US is likely to reach on its own by 2030. Growth is not solely constrained by the US. Sweden's data center usage is expected to double by 2030 and double again by 2040. The situation in the UK is similar, with a five-fold growth predicted within the next decade. By 2030, it is expected that data centers will account for approximately 8% of global electricity usage, driven primarily by the increasing demands of AI.

Introduction of the AI Factory Implementing Next-Gen 800 VDC Architecture

Today's existing data center architecture uses traditional 54 V in-rack power distribution and is limited to a few hundred kilowatts (kW). Bulky copper busbars are required to transfer this low-voltage electricity from the rack-mounted power shelves to the compute trays. As power increases above 200 kW, this architecture encounters physical limitations due to power density, copper requirements, and reduced system efficiency.

With the emergence of the 'AI factory,' a new class of data center purpose-built for large-scale, synchronous AI and high-performance computing (HPC) workloads has introduced a set of challenges in power architecture. Traditional enterprise and cloud data centers can no longer meet the multi-megawatt rack densities required by today's accelerated computing platforms. These challenges call for a fundamental architectural shift.

Next-generation AI factories will require gigawatts (GW) of power for the increasing demand for AI computation. Due to the higher voltage level of 800 VDC, the thickness of copper wires can be reduced by up to 45%, as I2R losses are minimized, allowing the same amount of power to be delivered with increased voltage and lower current. Using a traditional 54V DC system, over 200 kg of copper would be required to power a 1MW rack, which is not sustainable for next-generation AI data centers with a power demand of several gigawatts.

The 800 VDC directly powers the IT racks (eliminating the need for additional AC-DC converters) and is converted by DC-DC converters to lower voltages, which drives the GPUs. Additionally, this new architecture will improve end-to-end power efficiency by up to 5%, reduce maintenance costs by 70% (due to fewer PSU failures), and lower cooling costs by directly connecting VDC to the IT and computing racks.

NVIDIA is at the forefront of next-generation data center power architecture, adopting 800 VDC as the new benchmark for high-density AI computing infrastructure.

800 VDC Power Distribution Provides:

- Higher efficiency by reducing resistive losses and copper usage.
- Scalable infrastructure to deliver MW-scale rack power with highly compact solutions.
- Global alignment with the IEC's low-voltage DC (LVDC) classification (≤1,500 VDC)
- Simplified power distribution with efficient thermal management

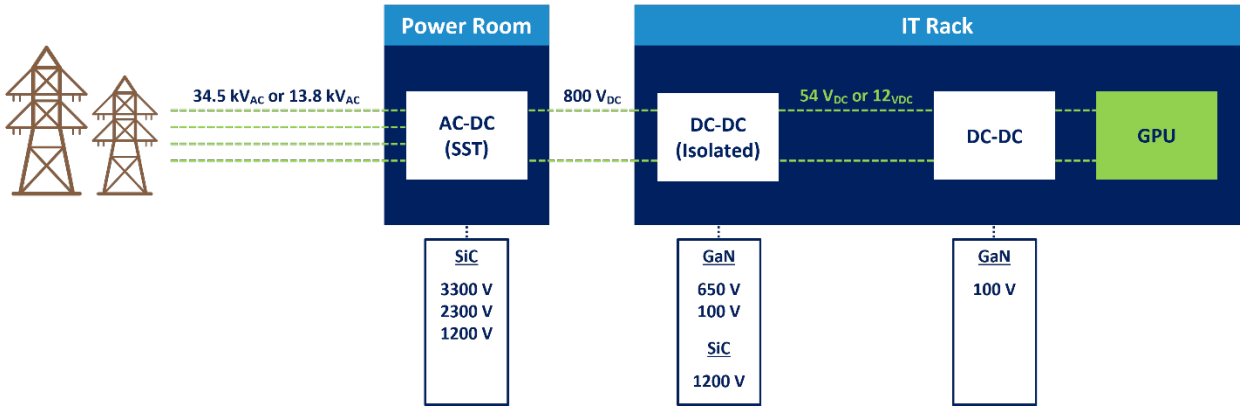


Figure 1: From the grid to the GPU, Navitas' advanced GaN and SiC technologies power every stage of the AI data center

Wide-Bandgap (WBG) Power Semiconductors Are Essential for Realizing an 800 VDC Architecture

Silicon has been dominant for many years but is approaching its performance limits in an increasing number of existing and emerging applications. Because WBG semiconductors, such as GaN and SiC, can withstand higher electric fields, they can sustain higher voltages and offer lower resistance per unit area, which is critical to achieving higher power density and efficiency. They can also operate at higher switching frequencies. The latter not only supports improved performance but also minimizes filtering requirements and allows the use of smaller external components (faster switching means energy is delivered in smaller packets and, therefore, less energy needs to be stored in the circuit's passive and inductive devices).

When compared to legacy silicon, these factors translate into several benefits, including smaller, faster, more efficient, and more reliable power electronics systems. Higher voltage capabilities open up opportunities in higher power designs, while dramatically improved efficiencies enable the same performance in smaller form factors or allow for enhanced performance in the same form factor.

However, multiple challenges exist in increasing power densities, with higher-density power supplies requiring increased thermal management, including heat dissipation, which adds cost and increases energy consumption. As densities increase, so do conversion efficiencies, and with this comes a reduced need for thermal management. These increases can be achieved through higher switching frequencies[1], but a fundamental issue in doing so is that silicon has reached its performance limits[2]. In high-density CRPS applications, replacing silicon MOSFETs and IGBTs with GaN and SiC devices enables significantly higher switching frequencies.

Navitas and NVIDIA are collaborating to develop advanced, next-generation, clean energy, wide-bandgap power semiconductors, such as medium- and high-voltage GaN and SiC power devices, to enable 800 VDC power architecture for next-generation AI factory computing platforms, ensuring greater power density, efficiency, reliability, and scalability.

Power Room – 34.5kV or 13.8kV MVAC Grid to 800 VDC Conversion: Ultra-High Voltage SiC Leads

Conventional power distribution architecture for data centers involves multi-stage power conversion, including the use of bulky and lossy line frequency transformers (LFTs), which step down the grid voltage from 34.5 kV or 13.8 kV MVAC 3-phase to 480 VAC 3-phase. This 480 VAC 3-phase is then subjected to multiple stages of power conversion to generate the required DC voltage (e.g., 54 VDC).

This approach introduces inefficiencies and increases the complexity of the system. By converting 34.5 kV or 13.8 kV MVAC 3-phase grid-power directly to 800 VDC using solid-state transformers (SST), a state-of-the-art power conversion technology enabled by high-voltage (HV) SiC power semiconductor devices, most intermediate conversion steps are eliminated. This streamlined approach minimizes energy losses, which typically occur during multiple AC/DC and DC/DC transformations.

With a single-step AC/DC conversion, the system benefits from a more direct and efficient power flow, reducing electrical complexity and maintenance needs. SST technology also offers better voltage stability and fault management, ensuring consistent power delivery to critical infrastructure. This approach also significantly reduces the number of power supply units (PSUs) with fans needed with the conventional approach. Fewer PSUs and fans lead to higher system reliability, lower heat dissipation, and improved energy efficiency, making VDC distribution a more effective solution for AI data centers.

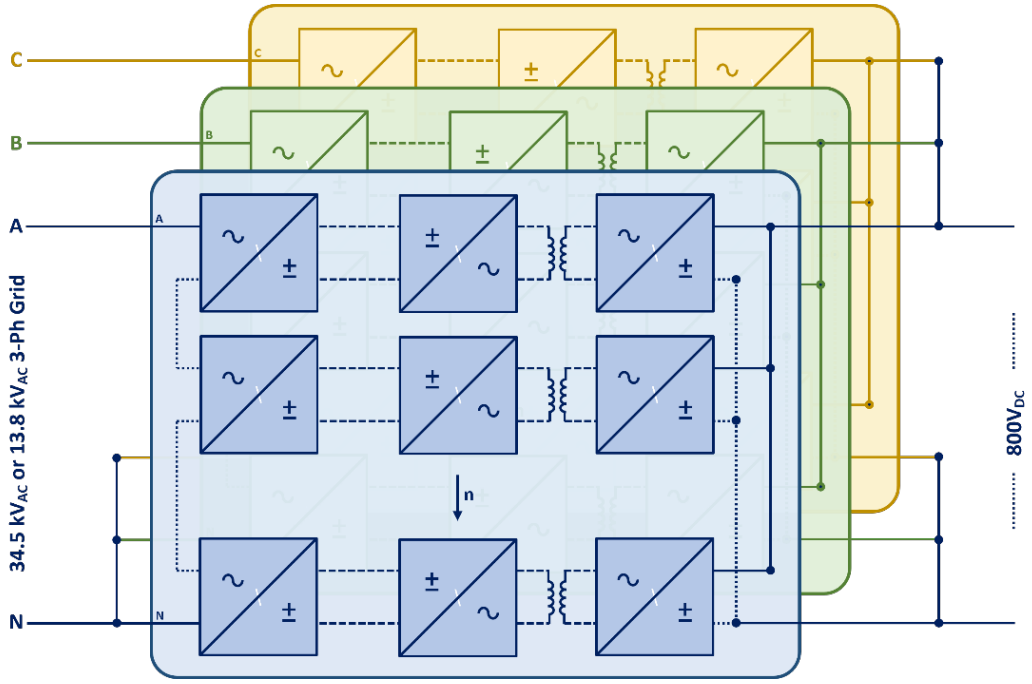


Figure 2: Typical solid-state transformer (SST) architecture for 34.5 kV or 13.8 kV MVAC to 800 VDC conversion

Enabled by over 20 years of SiC innovation leadership, GeneSiC™ trench-assisted planar MOSFETs and Schottky MPS™ diodes have been at the forefront of silicon carbide (SiC) technology. The HV SiC technology has been involved with over 20 government-funded projects, pushing the boundaries of performance, ruggedness, and reliability. These include funding from the U.S. Department of Energy (DoE) that led to the development of 3300 V and 6500 V SiC MOSFETs and monolithically-integrated SiC JBS-FETs for grid-tied power converter applications, government funding to develop 15 kV SiC MOSFETs for pulsed power applications, and funding from NASA to develop 500°C operating temperature capable SiC super-junction transistors for space exploration missions.

GeneSiC™ proprietary trench-assisted planar SiC MOSFET technology is a key enabler for efficient and reliable new-generation solid-state transformer (SST) designs. Fig. 2 shows the system architecture of a typical SST based on input-series output-parallel (ISOP) modular design approach, which enables scalable voltage and power. 3300 V and 2300 V SiC MOSFET discrete and power module solutions enable simpler design of the power converter stacks on the grid-input side (34.5 kV or 13.8kV MVAC).

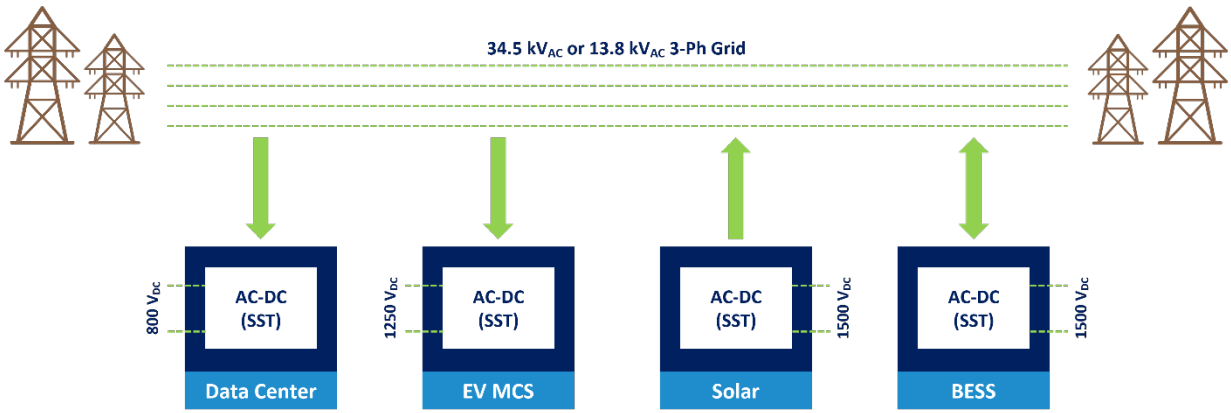


Figure 3: SST technology fueled by AI data centers set to modernize grid-infrastructure across battery energy storage systems (BESS), EV megawatt charging systems (MCS), and renewable energy

GeneSiC™ Trench-Assisted Planar SiC MOSFET Technology

Navitas Semiconductor, under its GeneSiC™ SiC MOSFET product line, utilizes a proprietary **trench-assisted planar technology**. This advanced design aims to deliver a "no-compromise" solution, balancing performance, manufacturability, and reliability in a way that traditional planar-gate or trench-gate SiC MOSFET designs often struggle to achieve. Although a trench-gate SiC MOSFET has a potential of lower specific on-resistance ($R_{ON,SP}$), it compromises with reliability and robustness and requires about 40% more process steps than a planar-gate SiC MOSFET, thus increasing the cost and lowering the yield.

Navitas' patented trench-assisted planar gate design is a no-compromise, next-generation solution; high-yield manufacturing, fast and cool operation, and extended, long-life reliability. It enables the lowest $R_{DS,ON}$ at high temperature, and the lowest energy losses at high speeds. This enables unprecedented, industry-leading levels of performance, robustness, and quality.

Trench-assisted planar technology demonstrates superior current spreading, a benefit attributed to the multi-step profile enabled by the trench-assist feature, as shown in Fig. 4. The design has been optimized to achieve lower $R_{DS,ON}$, even at elevated operating temperatures, which presents a significant advantage, as $R_{DS,ON}$ typically increases with temperature in SiC MOSFETs. By maintaining a lower $R_{DS,ON}$ across the operating temperature range, conduction losses are reduced, leading to cooler operation and higher system efficiency. This improved performance is partly due to the enhanced current spreading facilitated by the trench-assist's multi-step profile.

The referenced white-paper provides an in-depth explanation of trench-assisted planar technology and compares it with traditional-planar and advanced-trench SiC MOSFET technologies. Fig. 5 shows that **trench-assisted planar technology** delivers the industry's lowest $R_{DS,ON}$ shift with temperature – up to 20% lower $R_{DS,ON}$ at hot temperatures when compared with competing planar and advanced-trench SiC MOSFET technologies.

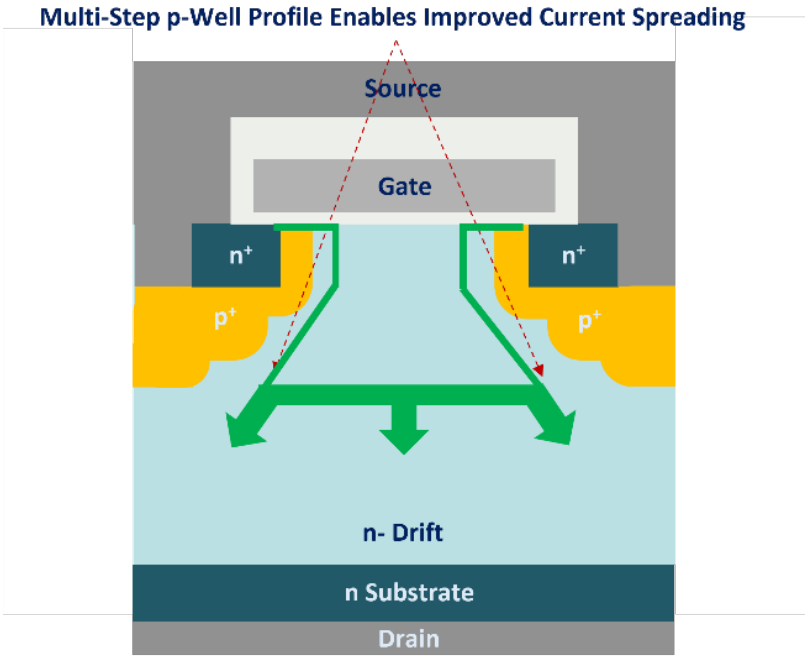


Figure 4: Multi-step profile enabled by proprietary trench-assist feature provides superior current spreading in the SiC MOSFET cell

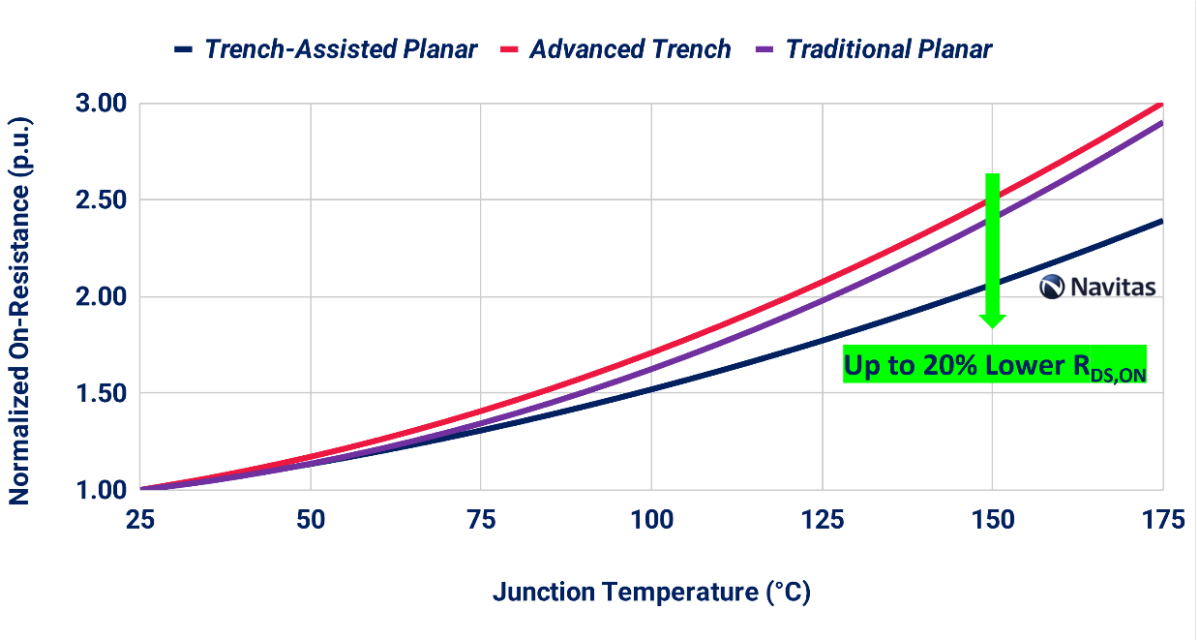


Figure 5: Benchmark of commercially available 2300 V and 2000 V SiC MOSFET technologies showcase GeneSiC™ trench-assisted planar technology offering up to 20% lower $R_{DS,ON}$ at elevated temperatures

For applications like SST that power mission-critical infrastructure with over 20 years of continuous operation, system failure is not an option. This requires a SiC MOSFET technology that guarantees robust and reliable operation for over 20 years of system lifetime. GeneSiC™ trench-assisted planar SiC MOSFET products offer an industry-first 'AEC-Plus' grade qualification – a new and extended reliability testing benchmark, defined by Navitas Semiconductor, that qualifies Navitas' products beyond the existing criteria listed under JEDEC and AEC-Q101 product qualification standards. his new benchmark showcases Navitas' deep understanding of system-level lifetime requirements and a strong commitment to enabling rigorously designed and validated products for demanding mission profiles in automotive and industrial applications. Key additions to this extended qualification include:

- Dynamic reverse bias (DRB) and dynamic gate switching (DGS) switching reliability tests
- Over 3x longer duration for static high-temperature, high-voltage tests (e.g. HTRB, HTGB)
- Over 2x longer power & temperature cycling
- 200°C qualification for relaxed thermal design margins and overload operation capability

As shown in Fig. 6, the multi-step profile enabled by the trench-assist feature provides a smoother distribution of electric-field (e-field) during the blocking state, resulting in the technology's ability to support 'AEC-Plus' reliability.

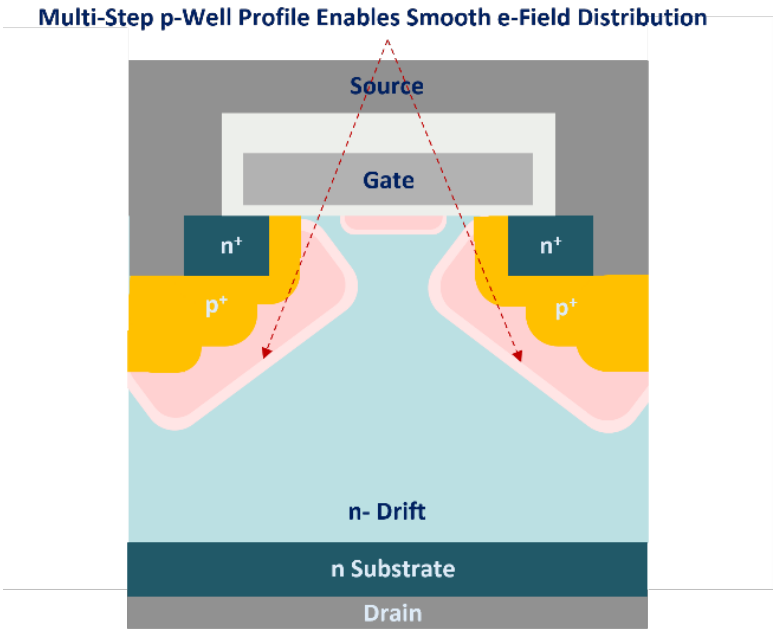


Figure 6: Multi-step profile enabled by proprietary trench-assist feature provides smoother distribution of electric field in the SiC MOSFET cell

As shown in Table 1, this rigorous 'AEC-Plus' testing includes advanced switching and extended static-reliability tests to meet the long-term mission-profile requirements of mission-critical applications.

'AEC-Plus' Qualification Tests	Navitas	Others
Extended Power Cycling	>30k cycles	7.5k to 15k cycles
Dynamic Reverse Bias	1000 hr to 3000 hr	No
Dynamic Gate Stress	>1.8 trillion cycles	Higher $V_{GS,TH}$ Shift
Dynamic HV-H3TRB	1000 hr	No
Extended HTRB	3000 hr	1000 hr
Extended HTGB & HTGB-R	3000 hr	1000 hr
HTRB at 200°C	1000 hr	0 hr at 200°C
HTGB & HTGB-R at 200°C	1000 hr	0 hr at 200°C
HV-H3TRB at 100% V_{DS}	1000 hr	V_{DS} = 80% Only

Table 1: Navitas benchmark 'AEC-Plus' grade reliability testing

By leveraging trench-assisted planar technology, Navitas SiC MOSFETs gain a significant advantage: they offer avalanche capability comparable to traditional planar technology and superior to trench technology, coupled with notably improved $R_{ON,SP}$, Q_{GD}× R_{ON} , and BV_{DSS}^2/ $R_{ON,SP}$ values compared to planar designs. Ultimately, these advancements provide Navitas devices with low static and dynamic resistance, fast switching speeds, and enhanced reliability and robustness over competitors. Referenced white-paper provides an in-depth comparison of the robustness of trench-assisted planar technology with traditional-planar and advanced-trench SiC MOSFET technologies.

Built to Endure: Advanced Epoxy-Resin Potting Technology for SiC Power Modules

Enabled by an advanced epoxy-resin potting technology, Navitas' new SiCPaK™ power modules are engineered to withstand high-humidity and high-temperature environments by preventing moisture ingression and enabling stable thermal performance by reducing degradation from power and temperature variations.

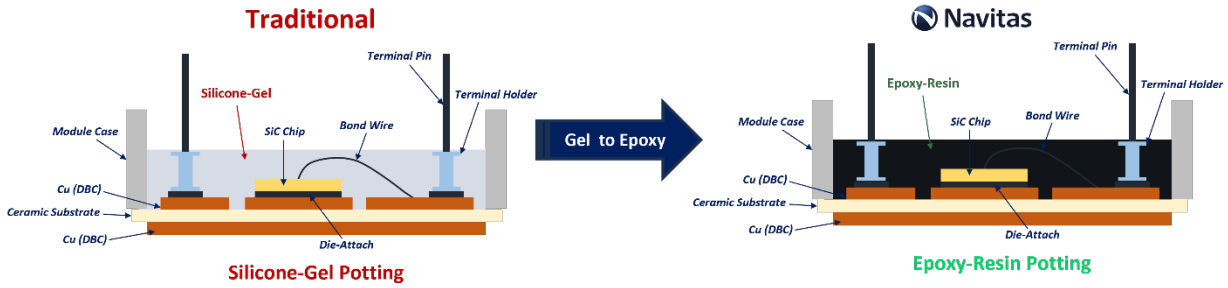


Figure 7: High-reliability power modules based on advanced epoxy-resin potting technology

As shown in Table 2, Navitas' epoxy-resin potting technology enables high endurance SiC power modules at multiple voltage classes (1200 V, 2300 V and 3300 V) that support over 10x longer lifetime for mission-critical applications.

Reliability Improvements	Navitas	Others
Temperature Humidity Bias	At module and SiC die level	At die level only
Temperature Cycling	> 1000 cycles	< 100 cycles
Thermal Shock Test	> 1000 cycles	< 100 cycles

Table 2: Reliability improvements with 'epoxy-resin potting' technology

Navitas' SiCPaK™ power modules demonstrated 5x lower thermal resistance shift (increase) following 1000 cycles of thermal shock testing (-40 C to + 125 C) compared to traditional silicone-gel-filled modules. Furthermore, all silicone-gel-filled modules failed isolation tests after 1000 cyles while SiCPaK™ epoxy-resin potted modules maintained acceptable isolation levels.

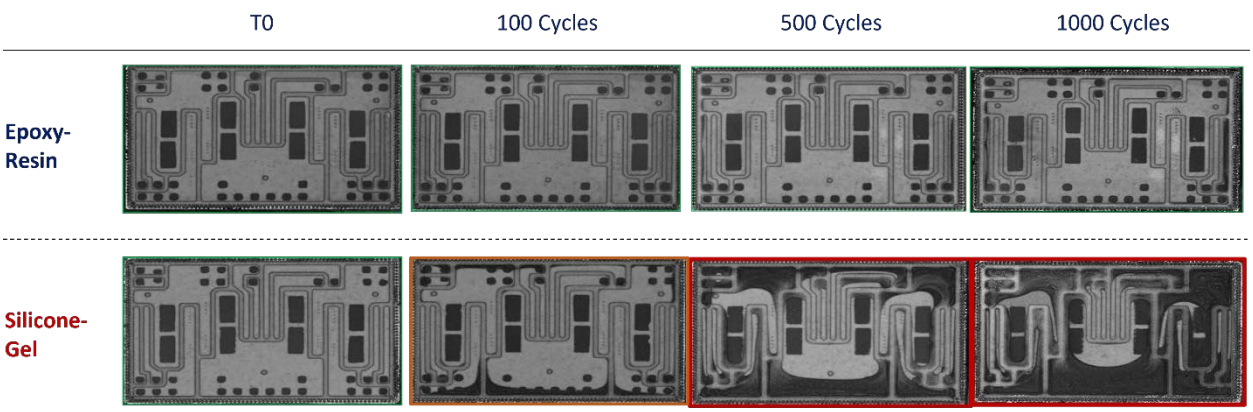


Figure 8: Thermal shock test results comparing epoxy-resin potting technology with traditional silicone-gel based potting in SiC power modules

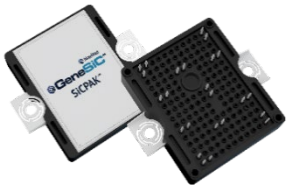
Roadmap to Next Generation SiC MOSFETs and Higher Voltage Classes up to 10 kV

Navitas' patented GeneSiC™ trench-assisted planar technology represents a significant leap forward in high voltage (HV) power electronics, providing a robust and reliable foundation for next-generation devices. This innovative architecture addresses the traditional trade-offs between performance, manufacturability, and ruggedness by leveraging a unique gate design that minimizes on-resistance while maximizing device reliability. This foundational technology has enabled the development of a comprehensive portfolio of power devices, ranging from commercial solutions at 2300 V , 3300 V and 6500 V, to advanced research and development efforts targeting the formidable 10 kV voltage classes.

To push the boundaries of performance even further, particularly for these demanding HV applications, on-going R&D is focused on combining the trench-assisted planar technology with innovative next generation device architectures. This approach is poised to overcome the inherent physical limitations of conventional designs. The synergistic integration of trench-assisted planar platform with next generation device architecture promises to deliver unprecedented improvements in the trade-off between breakdown voltage and on-resistance, enabling FoM improvements by over 30%, ultimately enabling superior power density, efficiency, and system reliability for the most critical high-voltage applications.

Navitas GeneSiC™ SiC MOSFET Product Line

	Power Discrete Solutions		
			
	Top Side Cooled SMD	**Bottom Side Cooled SMD**	**Through Hole**
650 V	9 mΩ - 55 mΩ	20 mΩ - 55 mΩ	9 mΩ - 55 mΩ
750 V	11 mΩ	-	11 mΩ
1200 V	7 mΩ to 135 mΩ	18 mΩ to 135 mΩ	7 mΩ to 75 mΩ
1700 V	-	375 mΩ	15 mΩ to 375 mΩ
2300 V	-	-	23 mΩ
3300 V	-	1000 mΩ	45 mΩ

	SiCPaK™ Power Module Solutions		
			
	Half-Bridge	**Full-Bridge**	**3L-NPC**
1200 V	5 mΩ to 17 mΩ	9 mΩ to 18 mΩ	9 mΩ
2300 V	5 mΩ to 11 mΩ	11 mΩ to 23 mΩ	-
3300 V	11 mΩ to 22 mΩ	22 mΩ to 45 mΩ	-

IT Rack: 800VDC to 54V/12VDC Conversion – GaN for Highest Power Density

By leveraging direct 800 V input, compute racks eliminate the need for integrated AC/DC conversion stages, simplifying the power architecture. These racks accept dual-conductor 800 V feeds and perform DC/DC conversion locally to power GPU systems. Removing bulky rack-level AC/DC converters frees up valuable space—enabling higher compute density and more efficient airflow. Compared to traditional AC-fed systems that require additional power modules, this streamlined approach reduces complexity, enhances system performance, and improves power delivery efficiency.

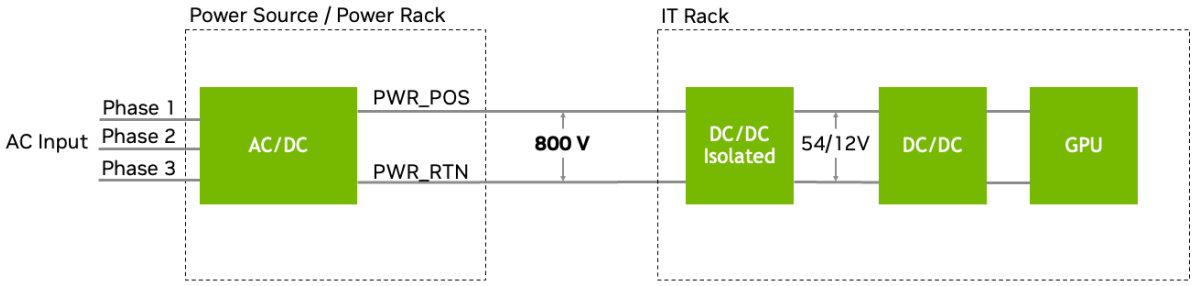


Figure 9: Direct 800 VDC to IT rack-level DC/DC conversion for GPU Power Delivery

Navitas 10 kW Full-Brick DC-DC Reference Design (800 VDC – 50 VDC)

Navitas created a high-power-density 10 kW DC-DC solution that converts 800V DC to 50V DC, including auxiliary power and control, within the dimensions of a full-brick (61 mm x 116 mm x 12 mm). It uses a 3-level half-bridge LLC resonant converter operating as a direct current transformer (DCX). The 3-level topology on the primary side reduces the voltage requirements by switching alternatively between ground, half input voltage, and full input voltage. This results in higher system efficiency. The LLC implements two inductors and a capacitor to function as a resonant converter, utilizing soft-switching techniques to provide the highest efficiency. This allows planar magnetics to offer maximum integration and the highest switching frequencies. The synchronous rectification stage activates the 100V GaN FETs to provide a low-conduction path while enabling the highest frequencies. Two SRs GaN FETs are parallelled to increase system power density.

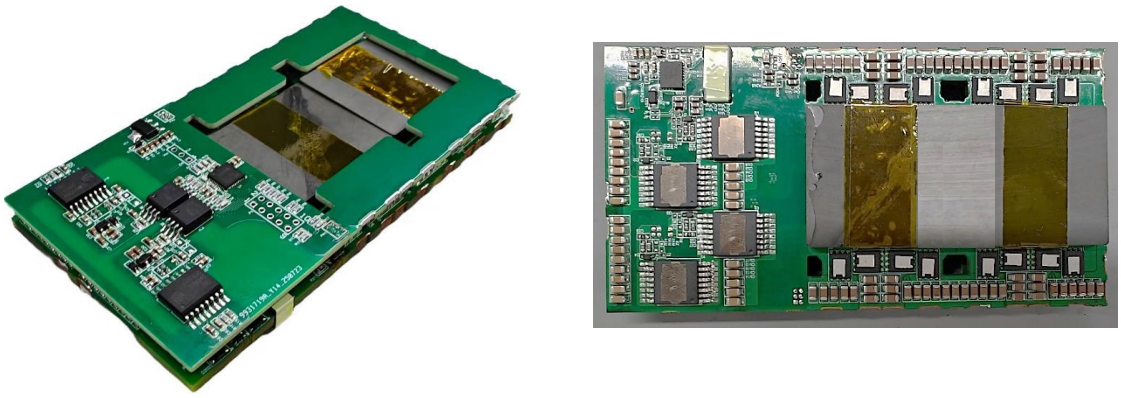


Figure 10: Navitas' 10kW, 800V-50V DC-DC full-brick solution, implements 100 V and 650 V GaN, enabling 1MHz switching frequency and 98% system efficiency

To deliver 10 kW at 50V necessitates a current output of 200 A. This requires multiple outputs when using LLC transformers to minimize the conduction loss of secondary windings and synchronous rectifiers (SRs). Building a multi-output LLC converter using GaN calls for a delicate balance between minimizing transformer winding losses, switching and conduction losses in the synchronous rectifiers, and power-supply termination losses. While raising the switching frequency is desirable to allow for smaller magnetic components, termination losses are increased.

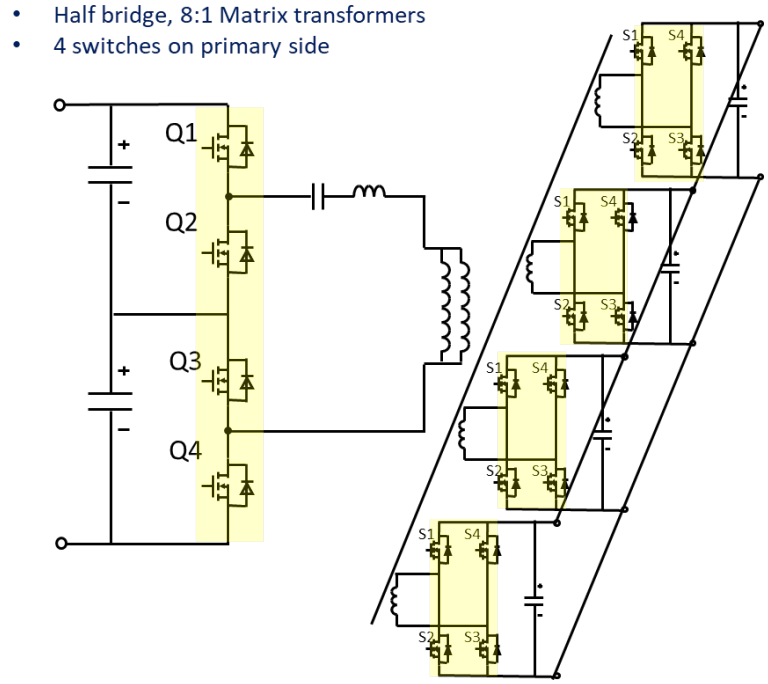


Figure 11: 3-Level Half-Bridge implements 8:1Matrix transformers, with 4 x 650V GaN FETs/GaNSafe on the primary side, and 16 x 100V GaN FETs on secondary/SR

Using multiple transformers can help avoid termination losses, albeit at the expense of a larger footprint. However, using multiple transformers introduces larger core losses and a larger magnetic size. Matrix transformers can mitigate these losses by ensuring flux cancellation between cores. A matrix transformer combines individual transformers such that primary side windings are connected in series/parallel while secondary side windings are connected in parallel/series. A configuration having primary-side series with secondary-side parallel connection is suitable for an LLC step-down application. When combined with high-frequency GaN devices, the planar transformer advantage is seen more clearly as they have a low voltage-second product that eliminates core saturation, thereby reducing overall losses.

Navitas GaNFast™ ICs and GaN FETs Maximize Power Density and Efficiency

Replacing silicon MOSFETs with GaN technology enables a significantly higher switching frequency, making it suitable for planar transformers while minimizing switching losses. GaN transistors also benefit from low conduction losses, due to their low channel resistance when turned on, as well as the absence of the intrinsic body diode present in silicon MOSFETs.

Enhancement-mode (normally-off) GaN FETs (or HEMTs: high electron-mobility transistors) have a relatively sensitive gate. Where MOSFETs can typically handle gate voltage from -10 V to 20 V, with a threshold of 2 V - 5 V, eMode GaN HEMTs have a gate voltage range of -10 V to 7 V. The GaN threshold voltage typically ranges from 1 V to 2 V.

GaN FETs thus require precise gate control. Therefore, attention must be provided when using discrete GaN FETs in high-power bridge circuits, as negative spikes in the gate-source voltage (VGS) at low-side turn-off can exceed the device's specified maximum. Additionally, the combined effects of gate-loop inductance and high di/dt can cause high-side and low-side VGS ringing, which poses a risk of shoot-through currents.

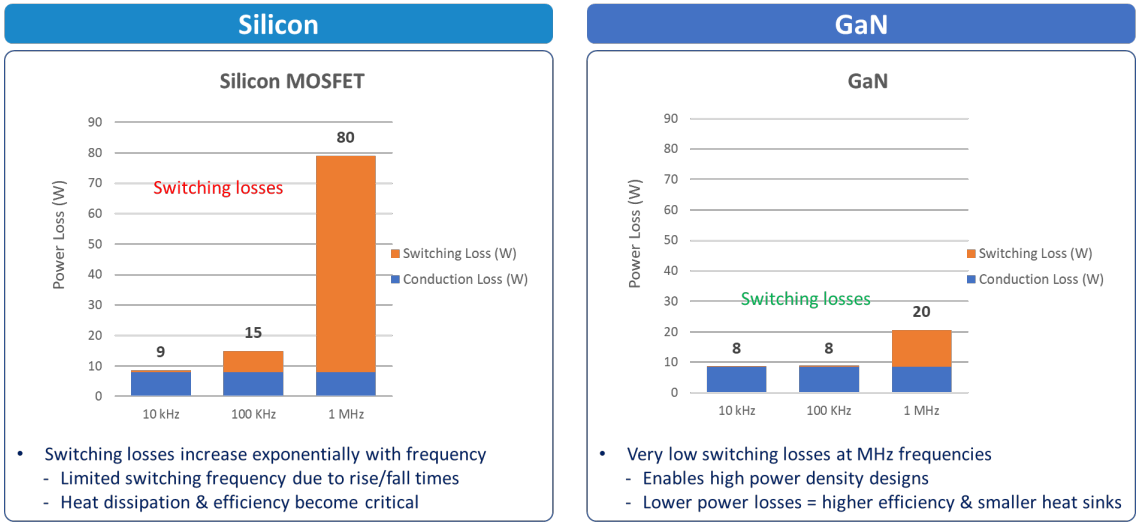


Figure 12: GaN enables MHz switching frequencies, enabling resulting in higher power density and efficiency than compared to silicon

Integrating an optimized gate driver in the same package as the GaN FET enables designers to control VGS, thereby mitigating these risks properly. Navitas' GaNSafe devices integrate the GaN FET and optimized gate-drive circuitry, incorporating advanced algorithms for dead-time control and additional safety features as needed. They enable a "digital in, power out" design approach with fast switching, high efficiency, and superior power density. They are conceived to meet the needs of AI-based data centers as well as EV, solar, and energy storage systems.

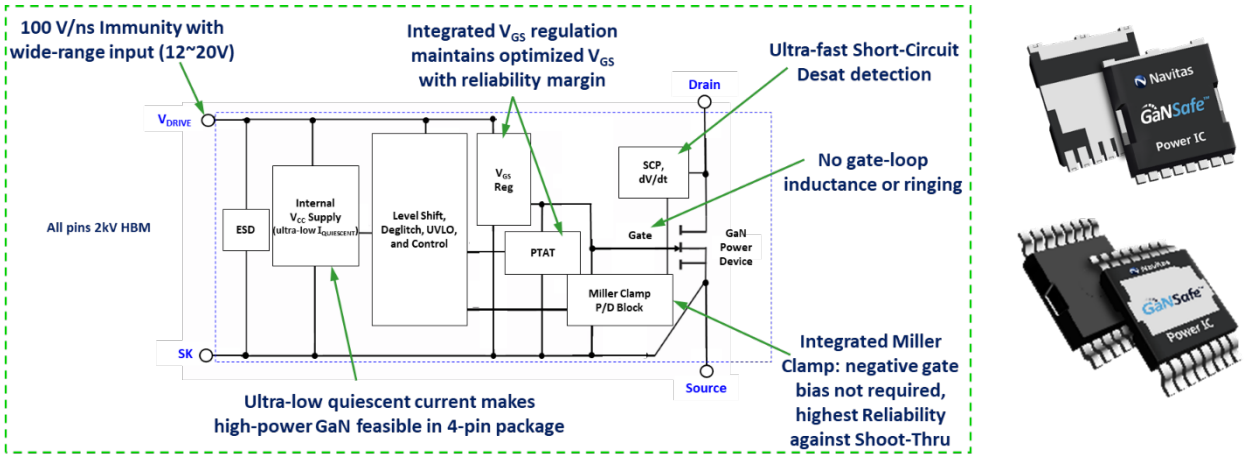


Figure 13: GaNSafe integrates short-circuit protection, negative gate-drive elimination, and programmable slew-rate control into a simple 4-pin device that functions like a discrete GaN FET without requiring VCC

Navitas integrated solutions, such as GaNSafe, offer zero gate-source loop inductance, which enables switching at up to 2 MHz to maximize application power density. High-speed short-circuit protection is built-in, with autonomous 'detect and protect' that acts within 50 ns. Electrostatic discharge (ESD) protection, typically not provided with discrete GaN transistors, is built-in and protects against events up to 2 kV. In addition, with 650 V continuous and 800 V transient voltage capability, they can survive extraordinary application conditions. Programmable turn-on and turn-off speed simplifies meeting EMI regulatory requirements. The devices have extremely low quiescent current and are housed in a 4-pin TOLL or TOLT packages, whereas comparable multi-chip modules can require up to three times as many connections and have poorer cooling capability.

The 650 V GaN portfolio also includes a new line of high-power discrete GaN FETs, starting from 11mOhms in TOLT package, offering industry standard packages for customers requiring multi-sourcing options.

Navitas' new 100 V GaN FET portfolio delivers industry-leading efficiency, power density, and thermal performance in advanced dual-sided cooled packages. These FETs are specifically optimized for the sync rectification FETs on the 54V output stage, or for the primary stage on the intermediate bus converter (IBC) where ultra-high density and thermal management are crucial for meeting the demands of next-generation AI compute platforms. The 100V GaN FETs are fabricated on a 200 mm GaN-on-Si process through a new strategic partnership with PSMC, enabling scalable, high-volume manufacturing.

Family	Part #	$V_{DS(CONT)}$ (V)	$V_{DS(TRANS)}$ (V)	$R_{DS(ON)typ.}$ (mΩ)	$R_{DS(ON)max.}$ (mΩ)	Current (A)	Package	ES	QS
GaNSafe™ Int. Drive + Protection	NV6511	650	800	70	98	22	 TOLL	Released	Released
	NV6512C			40	55	41			
	NV6513			32	45	53			
	NV6515			25	35	65			
	NV6514C			18	25	80			
	NV6522			40	55	41	 TOLT		
	NV6523			32	45	53			
	NV6525			25	35	65			
	NV6524			18	25	80			

Family	Part #	$V_{DS(CONT)}$ (V)	$R_{DS(ON)typ.}$ (mΩ)	$R_{DS(ON)max.}$ (mΩ)	Current (A)	Package	ES	QS
GaNFast™ FETs Discrete GaN	NV00810	100	0.8	1.0	165	PQFN5x6 DC	Q4'25	Q1'26
	NV01110		1.1	1.5	150		Q4'25	Q1'26
	NV02210		2.2	2.6	100		Q4'25	Q1'26
	NV6024	650	17	25	80	 TOLT	Q4'25	Q1'26
	NV6066		11	15	120		Q4'25	TBD

Figure 14: Navitas' GaN Portfolio Overview of GaNSafe™ Integrated Protection & GaNFast™ Discrete FETs for High-Performance Power Conversion

Conclusion

The exponential growth of AI workloads is transforming the data center landscape, creating unprecedented demands for power density, efficiency, and scalability. Traditional silicon-based power electronics and 54 V architectures are no longer sufficient to meet the multi-megawatt requirements of next-generation AI factories. The transition to an 800 VDC architecture, direct from grid to GPU, marks a fundamental inflection point, enabling MW rack-level power delivery, significant reductions in copper and cooling costs, and meaningful improvements in overall system efficiency.

Navitas' wide bandgap power technologies, GeneSiC™ MOSFETs for AC grid-to-800 VDC conversion, and GaNFast™ and GaNSafe™ devices for high-frequency, high-density DC-DC conversion, address the full chain of power delivery from grid to GPU. By combining advanced device physics, innovative packaging, and extended reliability standards, Navitas delivers robust, efficient, and scalable solutions purpose-built for AI factories.

Navitas is redefining data center power architecture, providing the foundation for next-generation AI infrastructure. By enabling compact, efficient, and reliable solutions, Navitas' GaN and SiC technologies ensure that future data centers can meet the world's growing compute demands.

References

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