

BDS EVB User Guide

BDS evaluation board to evaluate 650V Bi-Directional GaNFast™ Power Switch

1. Features

- For 650V Bi-Directional GaNFast power switches
- Driver has 4A peak source and 6A peak sink output current
- Simple Operation
- Small form factor
- Two separate dual-channel isolated gate driver
- Three separate driving power source

2. Applications

This board is to be used during engineering development or evaluation purpose only, for evaluation and measurement of the key features of the 650V Bi-Directional GaNFast™ Power Switch.

3. Description

This user guide explains how to operate the 650V Bi-Directional GaNFast™ evaluation board in TOLT package (Daughterboard) together with the Evaluation platform (Motherboard). It is intended to be used for double pulse testing to evaluate the switch characteristics and proof the data sheet specifications. Of course, it can also be extended to other topologies as needed to evaluate its characteristics.

4. Table of Contents

Contents

1. Features	1
2. Applications.....	1
3. Description	1
4. Table of Contents	2
5. Overview.....	4
6. Specifications	6
7. Usage together with motherboard	7
8. Schematic.....	10
9. Example circuit: Clamped Inductive Switching.....	12
10. Layout.....	15
11. Bill of materials	17
12. Revision history.....	18

IMPORTANT NOTICE:

Hazardous voltages are present on this demo board. Personal contact with high voltages may result in injury or death. Correct handling and safety procedures must be observed. Boards are for lab bench evaluation only. Not for installation in end-user equipment.

CAUTION:

This board contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

5. Overview

This platform was developed to show the optimal driving of the 650V Bi-Directional GaNFast™ in TOLT package. To achieve this target the design was split into two boards, one motherboard and a flexible daughterboard. The modular approach enables future expansion of the platform with additional daughterboard. This means, the daughter board is connected to the motherboard via connectors.

The daughterboard contains three separate driving power supplies, two isolated gate drivers to drive two 650V Bi-Directional GaNFast™ power switches in half-bridge configuration. Figure 1 and Figure 2 shows the daughterboard. Figure 3 and Figure 4 shows the motherboard evaluation platform.

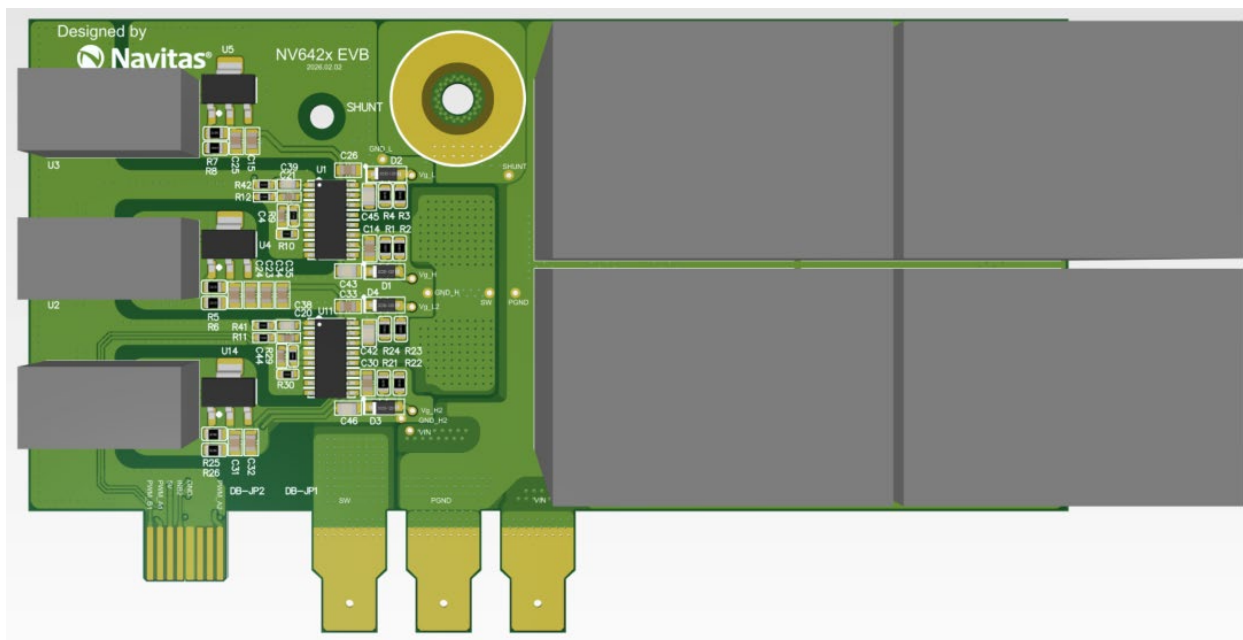


Figure1. Top view of daughterboard

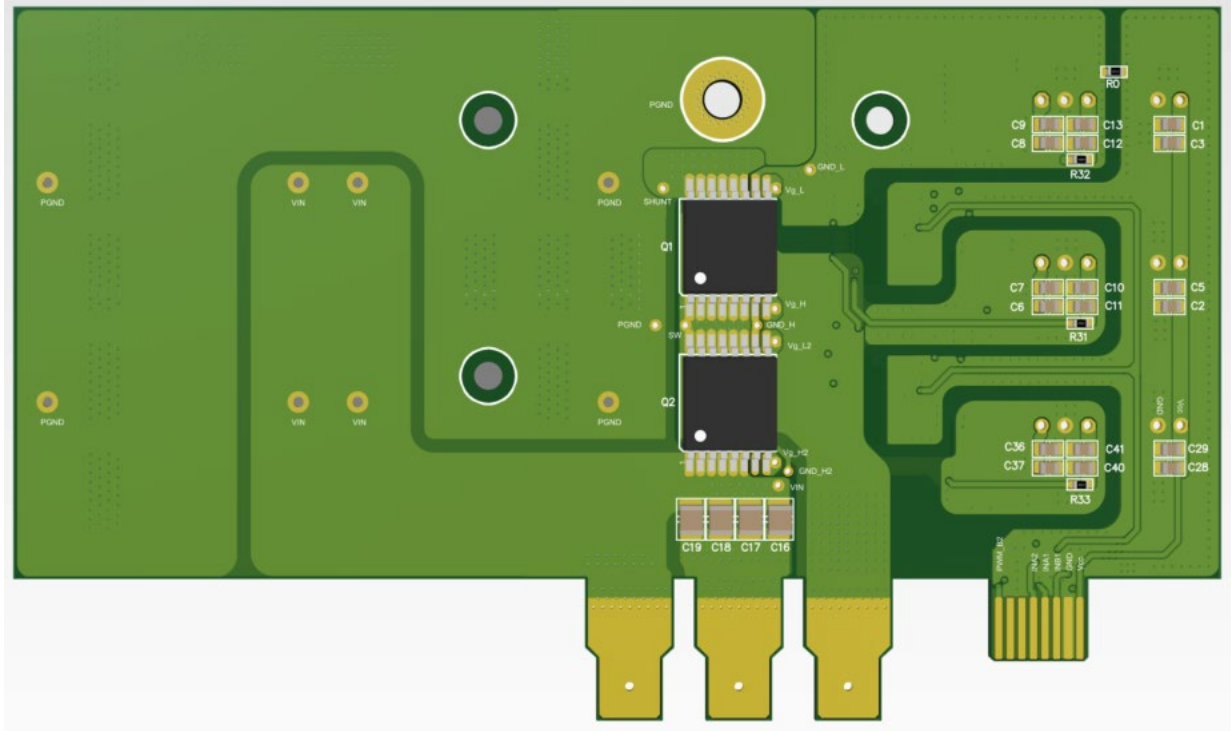


Figure2. Bottom view of daughterboard

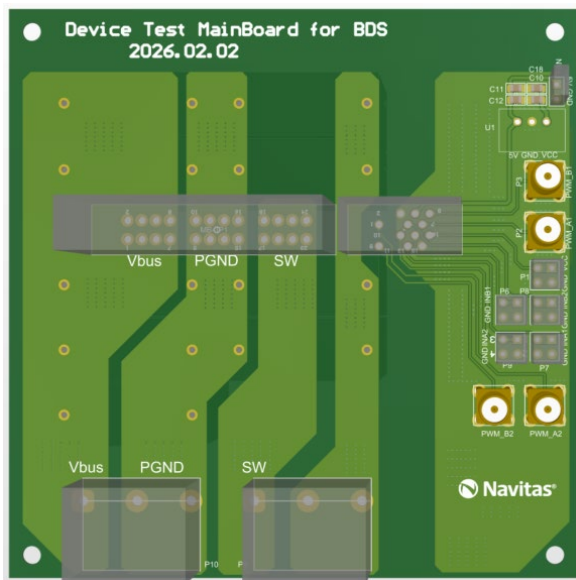


Figure3. Top view of motherboard

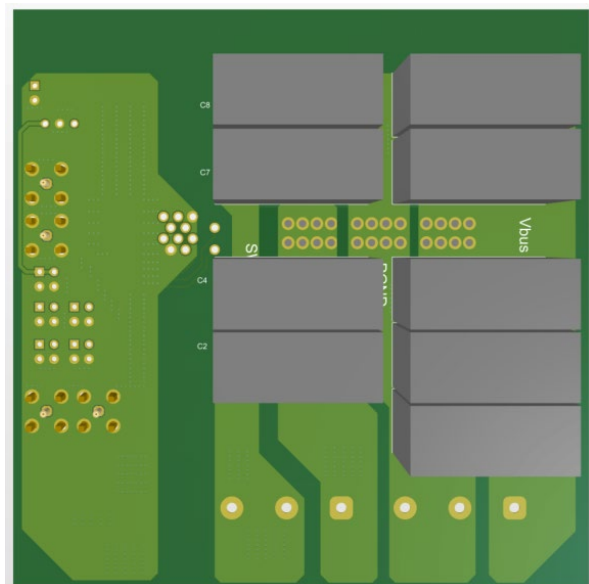


Figure4. Bottom view of motherboard

6. Specifications

The key specifications of this board are displayed in Table 1.

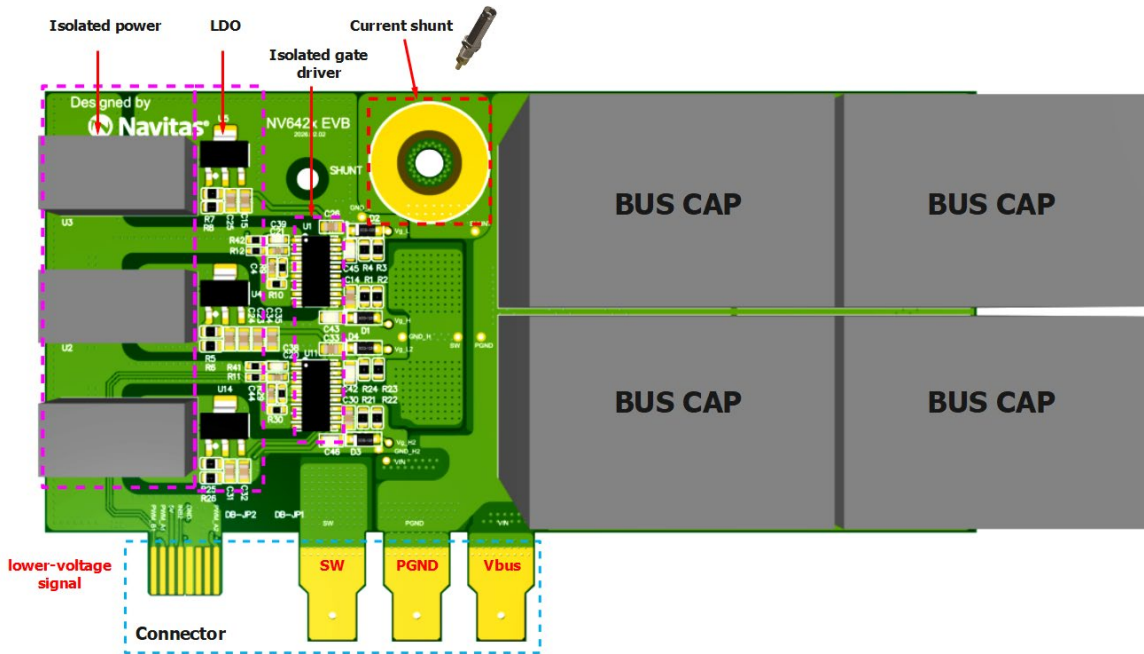
Table 1. Parameter

PARAMETER	SYMBOL	VALUE			UNITS
		Min.	Typ.	Max.	
Input DC Bus Voltage	V _{bus}	-	400	650	V
Supply Voltage	V _{cc}	13.5	15	16.5	V
PWM Input Pin Voltage	V _{pwm} ⁽¹⁾	3	-	18	V
High Level Input Threshold Voltage at PWM	V _{IH}	2	-	-	V
Low Level Input Threshold Voltage at PWM	V _{IL}	-	-	0.8	V
Positive Driver Output Voltage ⁽²⁾	V _{CC_H/L}	-	6	-	V
Negative Driver Output Voltage	V _{SS_H/L}	-	-3	0	V
Operating Ambient Temperature	T _a	-	25	-	°C
Mechanical dimensions Daughterboard	Length	-	140	-	mm
	Width	-	80	-	mm
Mechanical dimensions Motherboard	Length	-	100	-	mm
	Width	-	100	-	mm

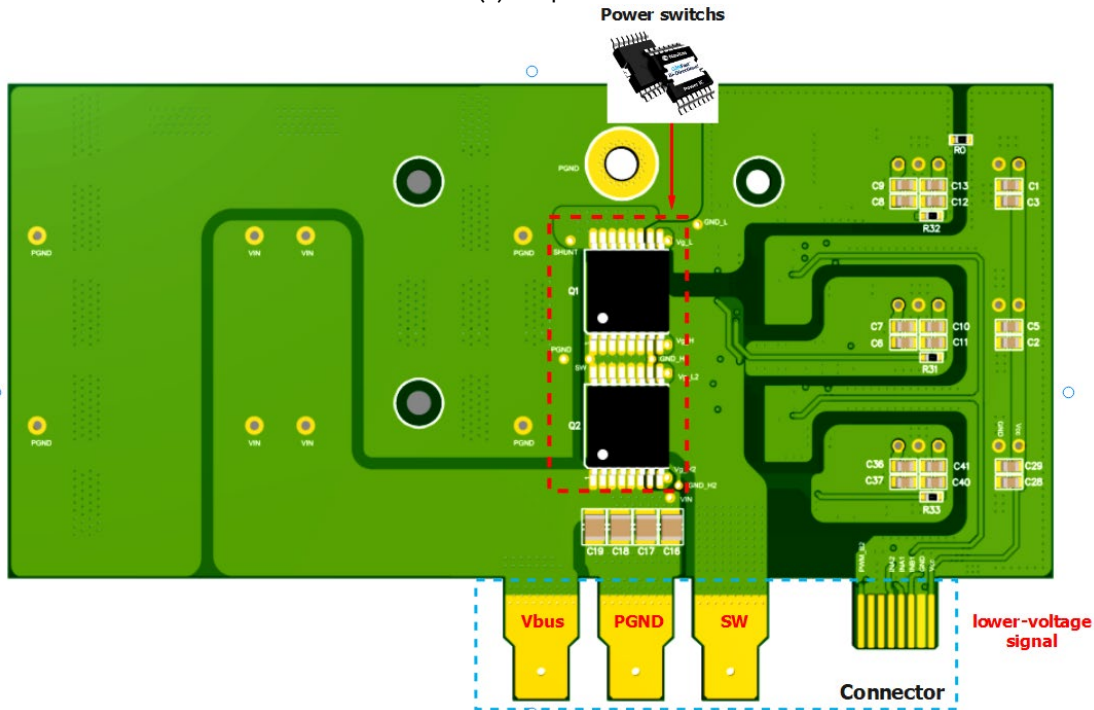
- (1) The PWM interface can be controlled by a pulse generator, a microcontroller, or other digital circuits.
- (2) According to user requirement, 6V drive voltage can be obtained by replacing the drive power supply and LDO.
- (3) Exposure to conditions beyond the maximum operating conditions for extended periods of time may affect device reliability.

7. Usage together with motherboard

The evaluation platform motherboard is used, commissioning is simple, as the daughterboard was specifically designed to be used together with it. Figures 5 and 6 show the function domains of this daughterboard and motherboard.



(a) Top view



(b) Bottom view

Figure 5. Function domains of the daughterboard

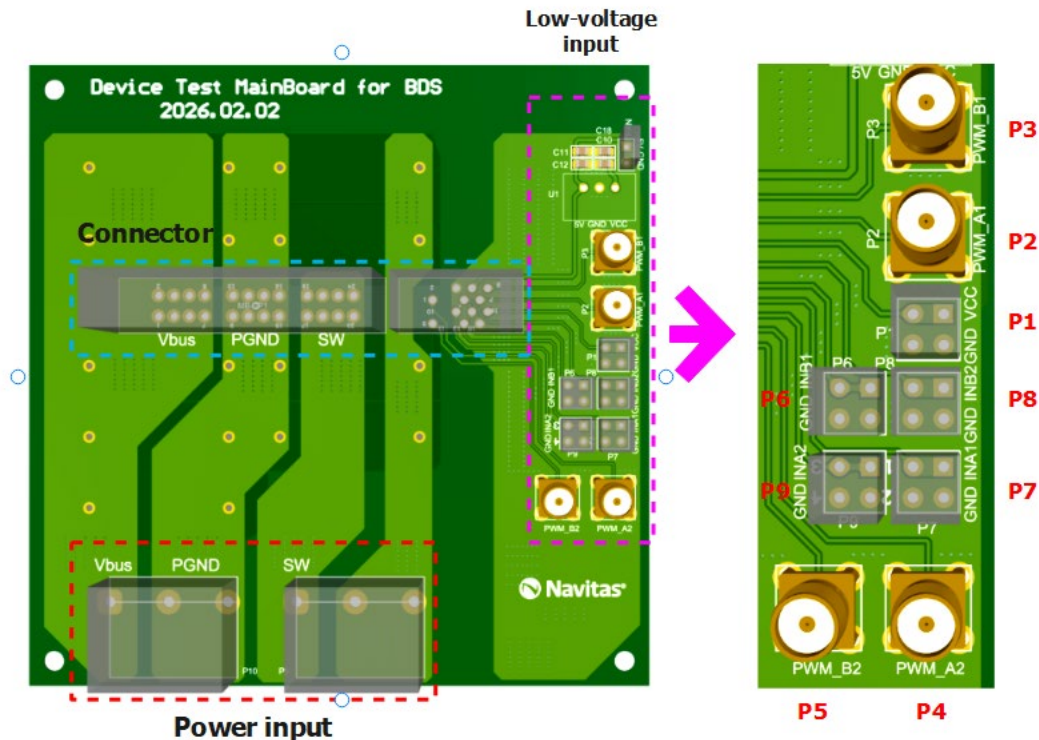


Figure 6. Function domains of the motherboard

The motherboard is divided into three sections: the low-voltage input side, power input side and connector. The low-voltage input side includes Vcc supply voltage input and PWM signal input. The PWM signal can be controlled by a pulse generator, a microcontroller, or other digital circuits. The power input side main includes V_{Bus} DC power input, switch node (SW), extended input interface Vo and power ground PGND. It can also be extended to other topologies as needed to evaluate its characteristics through the Vo interface. The connector is the only interface connected to the daughterboard. They are separated by the marker dotted line.

The daughterboard is divided into five sections: connector, 650V Bi-Directional GaNFast™ power switches, isolated gate driver IC, driving power supply (with LDO) and current shunt. The gate driver IC is dual-channel isolated gate driver, and the driver has 4A peak source output current. Three separate driving power sources and LDOs are combined to generate positive and negative driving voltage respectively to the upper and lower bridge power switching devices. Of course, the resistance and capacitor can also be adjusted to use 0V turn-off. A current shunt, e.g. [SSDN-10](#), [SSDN-015](#) and so on, is essential when the user want to observe the device current (Refer to figure 7). The current shunt is BNC interface, which can be connected with the oscilloscope to observe the device's current waveform. Content of delivery is the EVB packed in a box, excluding current shunt. The current shunt needs to be ordered separately. Users can reasonably choose different ranges of the current shunt

according to the size of the device current. The bus capacitors C51 to C54 are not soldered. The customer can decide whether to use them based on their requirements.



(a)

Figure 7. Current shunt [SSDN-10](#)

Pin assignment:

The motherboard evaluation PCB has several connectors to supply the board and to get different signals in or out.

Table 2 The main Pin definition

CONNECTOR	NAME	NOTE
P1	Vcc	LV Power supply for driver
P2	PWM_A1	PWM_A1 input Pin
P3	PWM_B1	PWM_B1 input Pin
P4	PWM_A2	PWM_A2 input Pin
P5	PWM_B2	PWM_B2 input Pin
P6	INB1	PWM_B1 filtered
P7	INA1	PWM_A1 filtered
P8	INB2	PWM_B2 filtered
P9	INA2	PWM_A2 filtered
FAN	5V	Output 5V/0.5A for external devices supply power, like cooling fan.

Note: An adequate bus capacitor is needed to ensure a stable power voltage between Vbus and PGND. If the board set is expanded into other circuits, in the event of continuous operation, the user needs to add an adequate heatsink to ensure proper cooling of the 650V Bi-Directional GaNFast™. The heatsink should have a safe distance with high voltage.

8. Schematic

Figure 9 and figure 10 show the drawing of the motherboard and daughterboard.

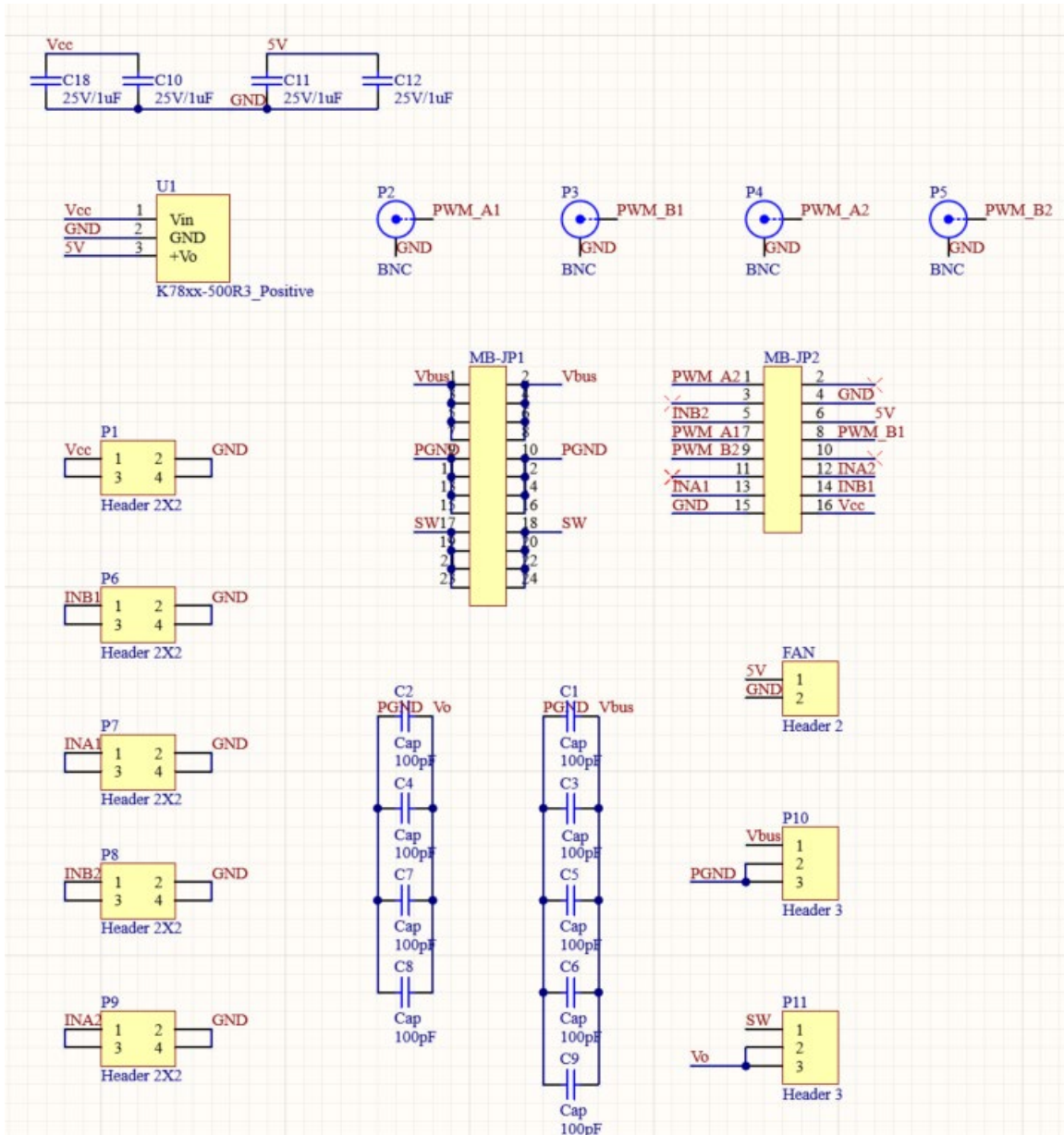


Figure 9. The motherboard schematic

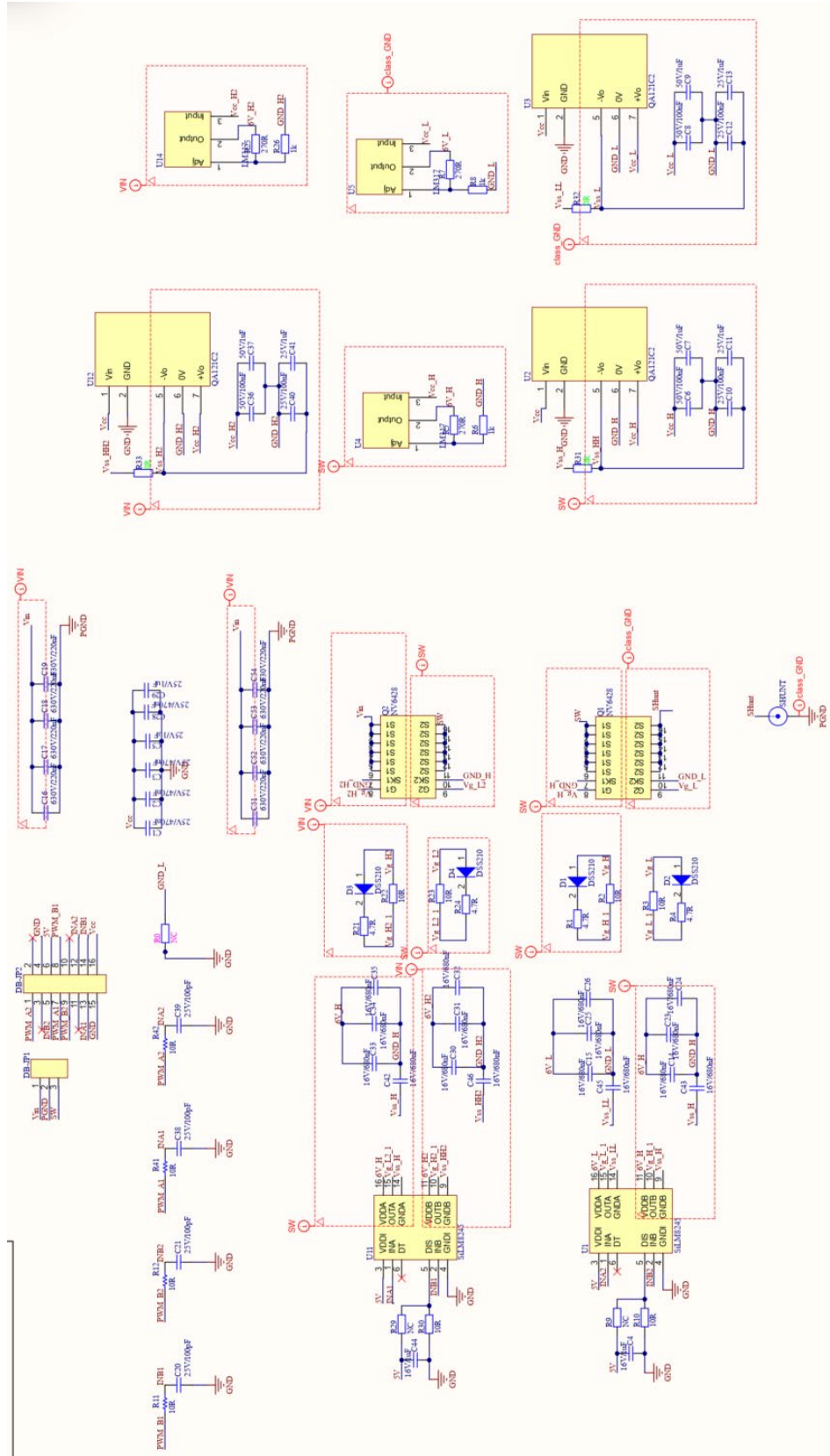


Figure 10. The daughterboard schematic

9. Example circuit: Clamped Inductive Switching

In the clamped inductive switching configuration, the inductor current builds up during each switching cycle. To prevent excessive current, PWM signals should not be generated continuously; instead, burst mode operation should be used to limit the number of applied cycles during testing.

This test configuration is particularly useful for evaluating circuit performance at higher currents without requiring a thermal management solution. The short pulse durations minimize power dissipation, reducing thermal stress on the system.

A simplified block diagram for this test is shown in Figure 11. To measure the device current more accurately by the current shunt, the switching device Q2 of the lower bridge is generally selected as the device under test.

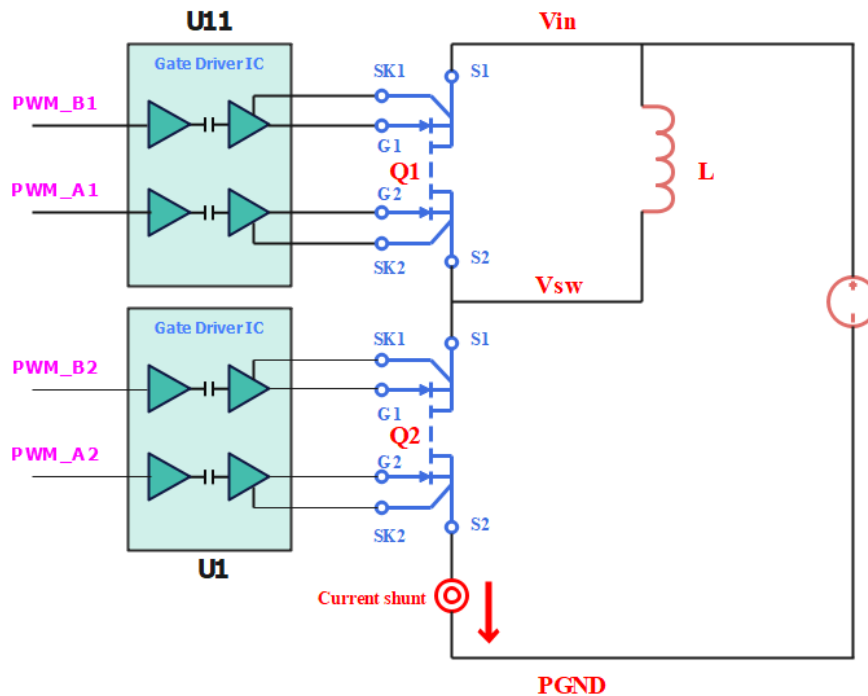


Figure 11. Clamped Inductive Switching Test Circuit

To start the operation these steps have to be taken:

- Take motherboard and daughterboard out of the box.
- Plug in the current shunt in the daughterboard.
- Plug in the daughterboard in the motherboard pin-to-pin.
- Plug in an adequate inductor between Vin and SW according to the test conditions.

- e) Connect the 15V LVDC source (ensure that it is switched off) to connector P1.
- f) Connect the PWM generator (ensure that it is switched off) to connector P2~P5.
- g) Connect the HVDC power (ensure that it is switched off) to Vin and PGND.
- h) Ready for pre-test and test.

Note: This board is equipped with measurement points. If the user wants to observe waveforms of different parameters, the board needs to be pre-processed and connect the probe at the corresponding position on the board.



Figure 12. PWM sequence for the test

It is important to note that in this test configuration, Q2 serves as the active device, with the inductor connected in parallel to Q1. Since Q1 and Q2 are bi-directional switches capable of blocking current in both directions, precise PWM sequencing is crucial to ensure proper current flow. For example, the PWM sequencing for the test circuit shown in Figure 12 is shown below. PWM_B1 and PWM_B2 for this example are biased as dc high. During the burst pulse sequence, PWM_A1 operates synchronously with PWM_A2 to minimize losses in the freewheeling device, Q1.

The PWM sequence illustrated above represents a burst of three pulses, but this logic can be extended to any number of pulses (N), provided that the safe operating area (SOA) limits of the active devices and the saturation current of the inductor are not exceeded. Example waveforms for this test are shown below in Figure 13.

In this test, 6 burst pulses are applied to the test circuit. CH1 shows the gate waveform G2 for the active device Q2. CH2 is the voltage across Q2 measured with a differential probe (from S1 to S2). CH3 shows the Q2 channel current. During this burst, the current builds up to a peak of 48A.

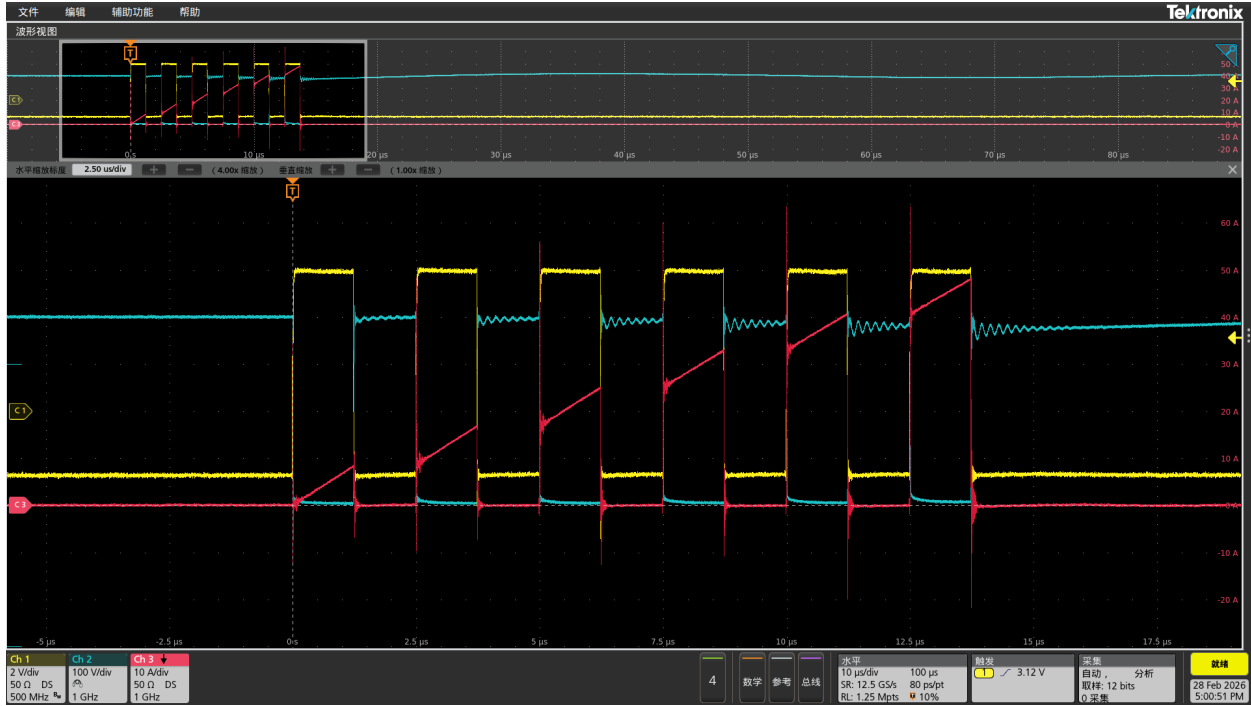
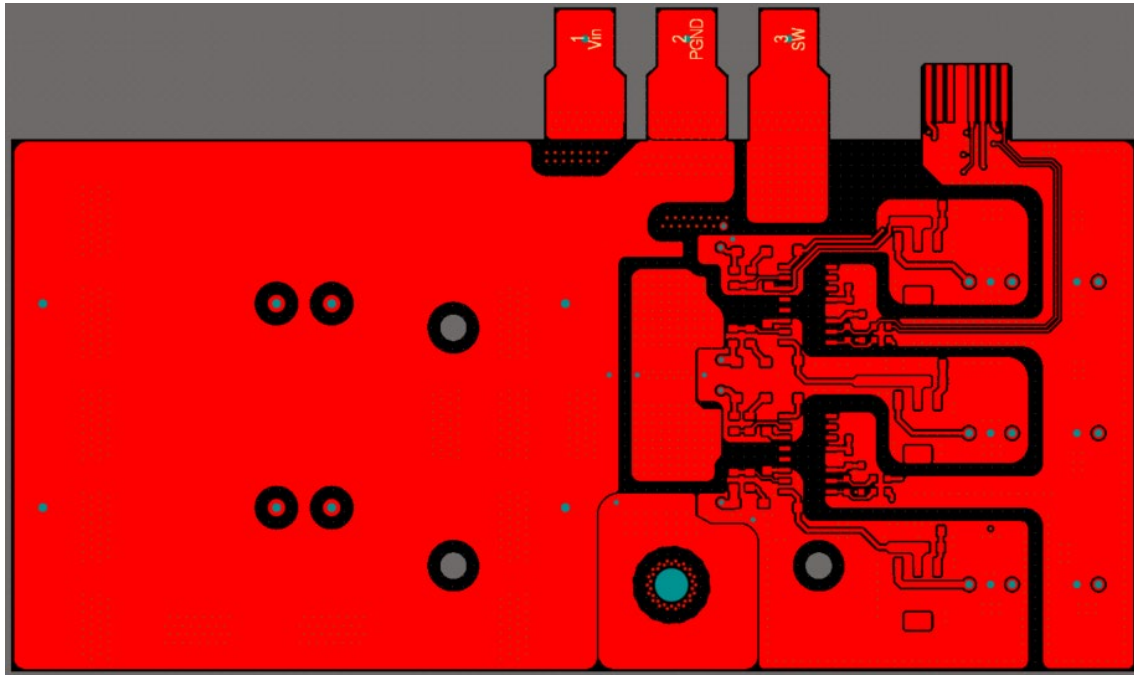


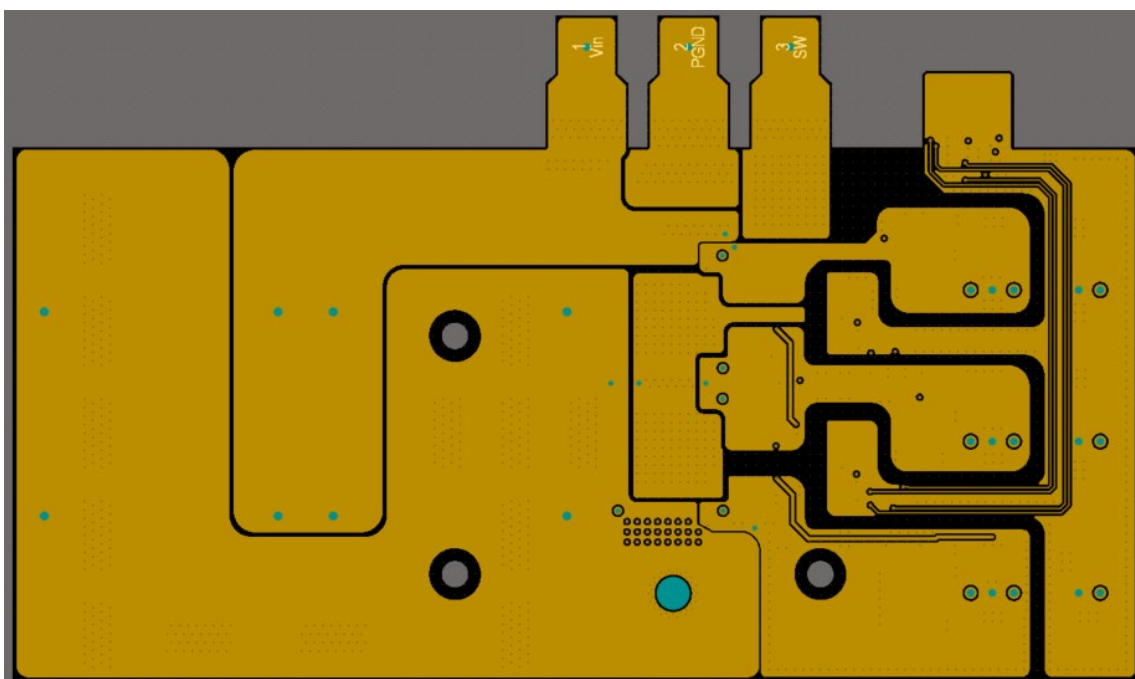
Figure 13. Clamped Inductive Switching Waveforms

10. Layout

The following figure 14 presents the different layers of the layout from the daughterboard. Due to the small dimensions of the design, a 4-layer layout was provided. The order from the top view: Top layer, Mid-Layer 1, Mid-Layer 2, bottom layer.



Top layer



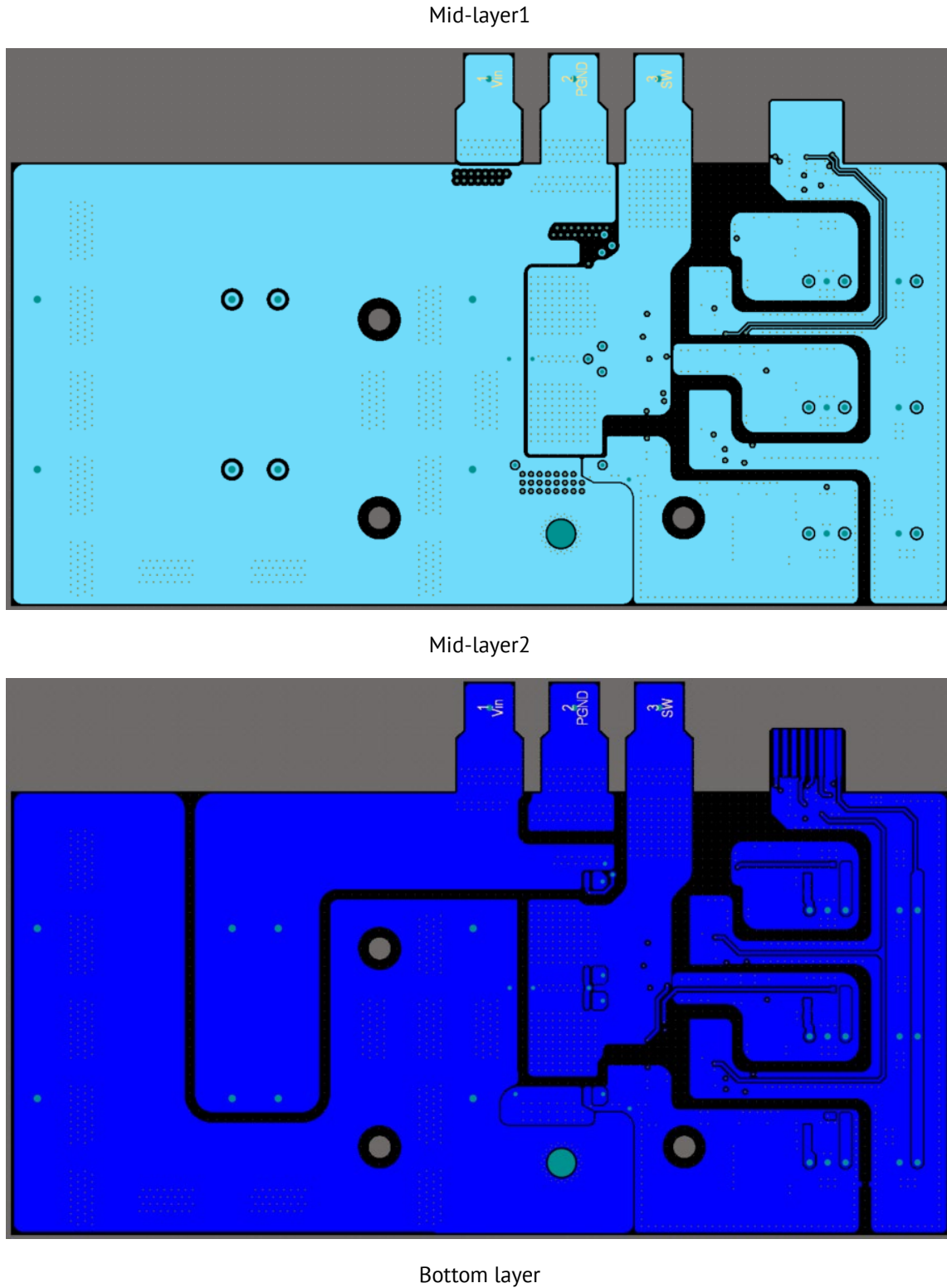


Figure 14. PCB Layout - Copper layers

11. Bill of materials

The bill of materials is only applicable to the 650V BDS daughterboard.

Comment	Designator	Description	Vendor	Part number	Quantity
25V/470nF	Cap, 470nF, 25V, 10%, 0805	C1, C2, C3, C28	YAGEO	CC0805KKX7R8BB474	4
25V/1uF	Cap, 1uF, 25V, 10%, 0805	C4, C5, C11, C13, C29, C41, C44	Vishay	VJ0805Y105KXXTW1BC	7
50V/100nF	Cap, 100nF, 50V, 10%, 0805	C6, C8, C36	Vishay	VJ0805Y104KXATW1BC	3
50V/1uF	Cap, 1uF, 50V, 10%, 0805	C7, C9, C37	YAGEO	CC0805KKX7R9BB105	3
25V/100nF	Cap, 100nF, 25V, 10%, 0805	C10, C12, C40	Vishay	VJ0805Y104KXXCW1BC	3
16V/680nF	Cap, 680nF, 16V, 20%, 0805	C14, C15, C23, C24, C25, C26, C30, C31, C32, C33, C34, C35, C42, C43, C45, C46	Vishay	VJ0805Y681MXJPW1BC	16
630V/150nF	Cap, 150nF, 630V, 10%, 0805	C16, C17, C18, C19	TDK	CGA6M1X7T2J154KTOY0N	4
25V/100pF	Cap, 100pF, 25V, 1%, 0805	C20, C21, C38, C39	Vishay	VJ0805D101FLXAJ	4
1kV/8uF	Cap, 8uF, 1kV, 5%, P=27.5mm	C51, C52, C53, C54	Faratron	C3D3A805JB00C00	4
DSS210	Diode, 100V, 2A, SOD-123FL	D1, D2, D3, D4	BORN	DSS210	4
NV6428	Navitas GaN Fet	Q1, Q2	Navitas	NV6428	2
4.7R	Res, 4R7, 1%, 0.5W, 0805	R1, R4, R21, R24	Vishay	CRCW08054R70FKEAHP	4
10R	Res, 10R, 1%, 0.5W, 0805	R2, R3, R22, R23, R11, R12, R41, R42, R10, R30	Vishay	CRCW080510R0FKEAHP	10
270R	Res, 270R, 10%, 0.25W, 0805	R5, R7, R25	YAGEO	SR0805KR-7W270RL	3
1k	Res, 1k, 10%, 0.25W, 0805	R6, R8, R26	YAGEO	SR0805KR-7W1KL	3
0R	Res, 0R, 0.125W, 0805	R31, R32, R33	Vishay	CRCW08050000Z0EB	3
2EDF7275F	Gate driver IC	U1, U11	Infineon	2EDF7275FXUMA1	2
QA01C-18	Driving supply	U2, U3, U12	MORSUN	QA01C-18	3
LM317	LDO	U4, U5, U14	TI	LM317DCYR	3

12. Revision history

Data	Status	Notes
Mar 9, 2026	Preliminary	Rev 1.1 Initial version

Additional Information

DISCLAIMER Navitas Semiconductor Inc. (Navitas) reserves the right to modify the products and/or specifications described herein at any time and at Navitas' sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied. This document is presented only as a guide and does not convey any license under intellectual property rights of Navitas or any third parties.

Navitas' products are not intended for use in applications involving extreme environmental conditions or in life support systems.

Products supplied under Navitas Terms and Conditions.

Navitas Semiconductor, Navitas, GaNFast, GaNSense and associated logos are registered trademarks of Navitas.

Copyright ©2024 Navitas Semiconductor Ltd. All rights reserved.



Navitas Semiconductor Ltd., 3520 Challenger St., Torrance, CA 90503, USA.

Contact: info@navitassemi.com